LYTSwitch-6 Family

Flyback CV/CC LED Driver IC with Integrated 650 V / 725 V MOSFET and FluxLink Feedback

Product Highlights

Highly Integrated, Compact Footprint

- Up to 94% efficiency across full load range
- Incorporates a multi-mode Quasi-Resonant (QR) / CCM flyback controller, 650 V or 725 V MOSFET, secondary-side control and synchronous rectification driver
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Exceptional CV/CC accuracy, independent of transformer design or external components
- Adjustable accurate output current sense using external sense resistor

EcoSmart™ – Energy Efficient

- Less than 15 mW no-load including line sense (without PF front end)
- Easily meets Energy Star and all global lighting energy efficiency regulations
- Low heat dissipation

Advanced Protection / Safety Features

- Input line OV with auto-restart
- Output fault OVP/UVP with auto-restart
- Open SR FET gate detection
- Input voltage monitor with accurate brown-in
- Thermal foldback ensures that power continues to be delivered (lower level) at elevated temperatures

Full Safety and Regulatory Compliance

- Reinforced insulation
- Isolation voltage >4000 VAC
- 100% production HIPOT compliance testing
- UL1577 and TUV (EN60950) safety approved

Green Package

- Halogen free and RoHS compliant

Applications

- Isolated off-line LED driver
- Smart LED lighting
- High-voltage flyback post regulator

Description

The LYTSwitch™-6 series family of ICs dramatically simplifies the development and manufacturing of off-line LED drivers, particularly those in compact enclosures or with high efficiency requirements. The LYTSwitch-6 architecture is revolutionary in that the devices incorporate both primary and secondary controllers, with sense elements and a safety-rated feedback mechanism into a single IC.

Close component proximity and innovative use of the integrated communication link, FluxLink, permit accurate control of a secondary-side synchronous rectification MOSFET with Quasi-Resonant switching of primary integrated high-voltage MOSFET to maintain high efficiency across the entire load range.

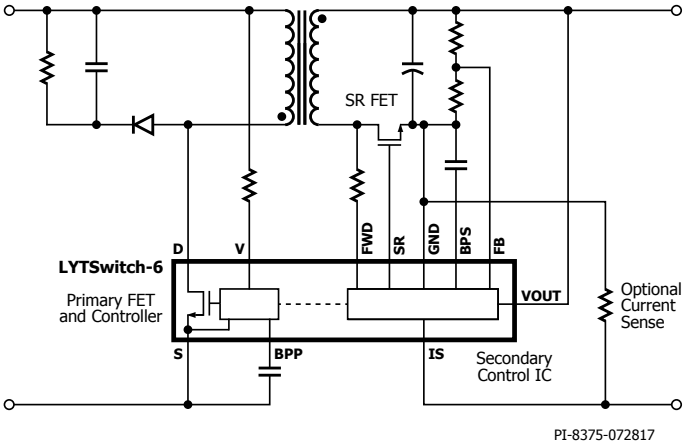


Figure 1. Typical Application/Performance.

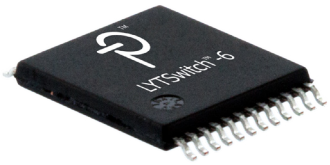


Figure 2. High Creepage, Safety-Compliant InSOP-24D Package.

Output Power Table

Product[3]	277 VAC ± 15%	85-305 VAC	380 VDC / 450 VDC[2]
	Open Frame[1]	**Open Frame[1]**	**Open Frame[1]**
LYT6063C/6073C	15 W	12 W	25 W
LYT6065C/6075C	30 W	25 W	40 W
LYT6067C/6077C	50 W	45 W	60 W
LYT6068C	65 W	55 W	

Table 1. Output Power Table.

Notes:

1. Minimum continuous power in a typical non-ventilated and PCB size measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < 125 °C.
2. With 725 V FET only.
3. Package: InSOP-24D.

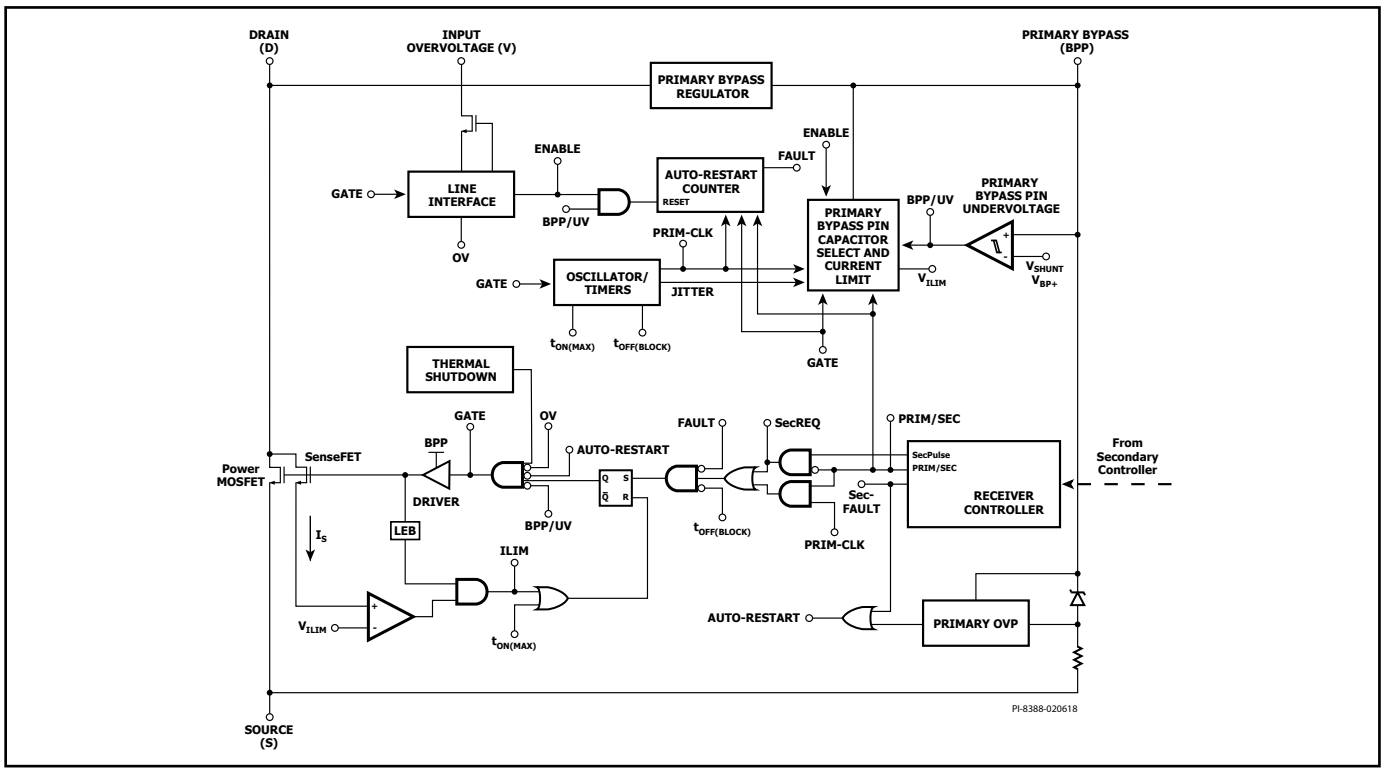


Figure 3. Primary Controller Block Diagram.

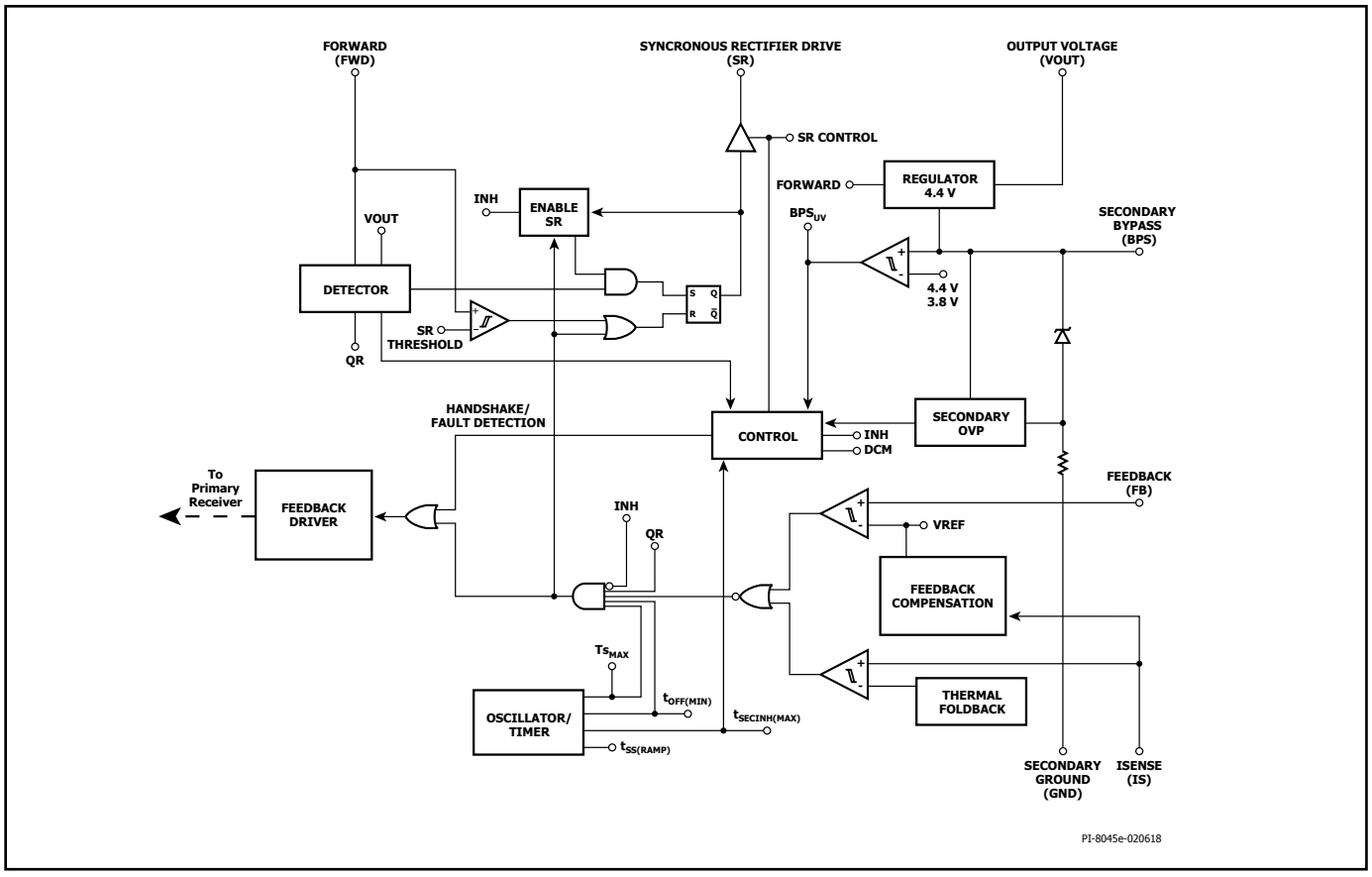


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply output terminals. An external current sense resistor should be connected between this and the GND pin. If current regulation is not required, this pin should be tied to the GND pin.

SECONDARY GROUND (GND) (Pin 2)
GND for the secondary IC. Note this is not the power supply output GND due to the presence of the sense resistor between this and the ISENSE pin.

FEEDBACK (FB) Pin (Pin 3)
Connection to an external resistor divider to set the power supply output voltage.

SECONDARY BYPASS (BPS) Pin (Pin 4)
Connection point for an external bypass capacitor for the secondary IC supply.

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 5)
Gate driver for external SR FET.

OUTPUT VOLTAGE (VOUT) Pin (Pin 6)
Connected directly to the output voltage to provide current for the controller on the secondary-side.

FORWARD (FWD) Pin (Pin 7)
The connection point to the switching node of the transformer output winding providing information on the primary switch timing. Provides power for the secondary-side controller when V_{OUT} is below a threshold.

NC Pin (Pin 8-12)
Leave open. Should not be connected to any other pins.

Input Overvoltage (V) Pin (Pin 13)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting overvoltage conditions at the power supply input. This pin should be tied to Source to disable OV protection.

PRIMARY BYPASS (BPP) Pin (Pin 14)
The connection point for an external bypass capacitor for the primary-side supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1.

NC Pin (Pin 15)
Leave open. Should not be connected to any other pins.

SOURCE (S) Pin (Pin 16-19)
These pins are the power MOSFET source connection. It is also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 24)
Power MOSFET drain connection.

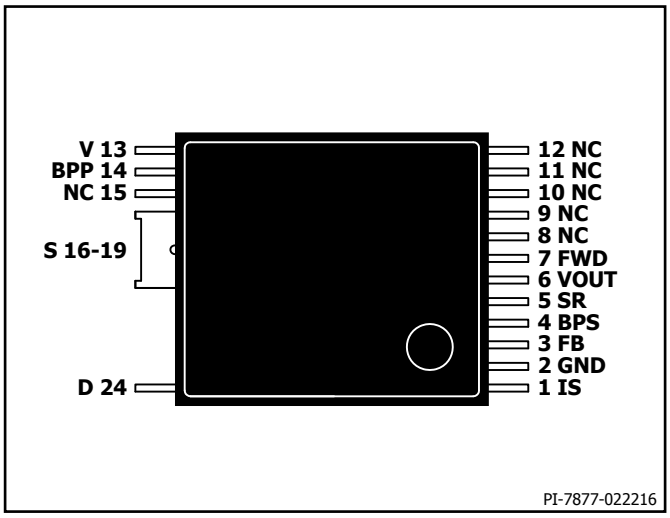


Figure 5. Pin Configuration.

LYTSwitch-6 Functional Description

The LYTSwitch-6 combines a high-voltage power MOSFET switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme using the package lead frame and bond wires to provide a safe, reliable, and low-cost means to communicate accurate direct sensing of the output voltage and output current on the secondary controller to the primary controller.

The primary controller on LYTSwitch-6 is a Quasi-Resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator; a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection, leading edge blanking, and a 650 V / 725 V power MOSFET.

The LYTSwitch-6 secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, a constant voltage (CV) and a constant current (CC) control circuit, a 4.4 V regulator on the secondary SECONDARY BYPASS pin, synchronous rectifier MOSFET driver, QR mode circuit, oscillator and timing functions, thermal foldback control and a host of integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller with the most important features.

Primary Controller

The LYTSwitch-6 features variable frequency QR controller + CCM operation for enhanced efficiency and extended output power capability.

PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the voltage on the DRAIN pin whenever the power MOSFET is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, there is a shunt regulator clamping the PRIMARY BYPASS pin voltage to V_{SHUNT} when the current is provided to the PRIMARY BYPASS pin through an external resistor. This facilitates powering the LYTSwitch-6 externally through a bias winding to decrease the no-load consumption to less than 15 mW.

Primary Bypass ILIM Programming

LYTSwitch-6 has user programmable current limit (ILIM) settings through the selection of PRIMARY BYPASS pin capacitor value. The PRIMARY BYPASS pin can use a ceramic capacitor for decoupling the internal supply of the device.

There are (2) programmable settings using 0.47 µF and 4.7 µF for standard and increased ILIM settings respectively.

Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power MOSFET when the PRIMARY BYPASS pin voltage drops below ~4.5 V (V_{BPP} - $V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise back to V_{SHUNT} to re-enable turn-on of the power MOSFET.

Primary Bypass Output Overvoltage Auto-Restart Function

The PRIMARY BYPASS pin has an OV protection non-latching feature. A Zener diode in parallel to the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding to activate this protection mechanism. In the event the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will disable the power MOSFET switching for a time $t_{AR(OFF)}$. After this time the controller will restart operation and attempt to return to regulation.

This VOUT OV protection is also available as an integrated feature on the secondary controller.

Over-Temperature Protection

The thermal shutdown circuitry senses the primary MOSFET die temperature. The threshold is typically set to T_{SD} with $T_{SD(H)}$ hysteresis. When the die temperature rises above this threshold the power MOSFET is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point it is re-enabled. A large hysteresis of $T_{SD(H)}$ is provided to prevent over-heating of the PCB due to continuous fault condition.

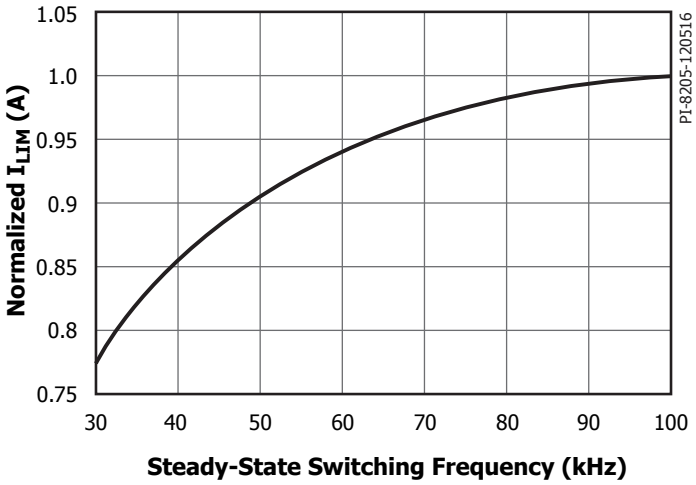


Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation

The primary-side controller has a current limit threshold ramp that is inversely proportional to time from the end of the last primary switching cycle (i.e. from the time the primary FET turns off at the end of a switching cycle).

The characteristic produces a primary current limit that increases as the load increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with immediate response when a feedback switching cycle request is received.

At high load, switching cycle have a maximum current approaching 100% ILIM gradually reduced to 30% of the full current limit as the load reduces. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise) but the time between switching cycles will continue to reduce as load reduces.

Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart

In the event a fault condition occurs such as an output overload, output short-circuit, or external component/pin fault, the LYTSwitch-6 enters into auto-restart (AR) operation. In auto-restart the power MOSFET switching is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency (~110 kHz) for longer than 80 ms.
2. No requests for switching cycles from the secondary for > $t_{AR(SK)}$.

The second was included to ensure that if communication is lost, the primary tries to restart again. Although this should never be the case in normal operation, this can be useful in the case of system ESD events for example where a loss of communication due to noise disturbing the secondary controller, the issue is resolved when the primary restarts after an auto-restart off time.

The very first auto-restart off-time is short. This short auto-restart timer is to provide a quick recovery under fast reset conditions. The short auto-restart off-time allows the controller to quickly check to determine whether the auto-restart condition is maintained beyond $t_{AR(OFF)SH}$. If so will resort to full auto-restart off timing.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection

In the event there are two consecutive cycles where the ILIM is reached within the blanking time and current limit delay time (~500 ns), the controller will skip approximately 2.5 cycles or ~25 µs (based on full frequency of 100 kHz). This provides sufficient time for reset of the transformer during start-up into large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring

The INPUT OVERVOLTAGE pin is used for input overvoltage sensing and protection.

A 4 MΩ resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the INPUT OVERVOLTAGE pin to enable this functionality. This pin functionality can be disabled by shorting INPUT OVERVOLTAGE pin to primary Source.

Primary/Secondary-Side Handshake

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

If the primary stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default into a start-up condition and attempt to detect handshake pulses from the secondary.

If the secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of SF FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

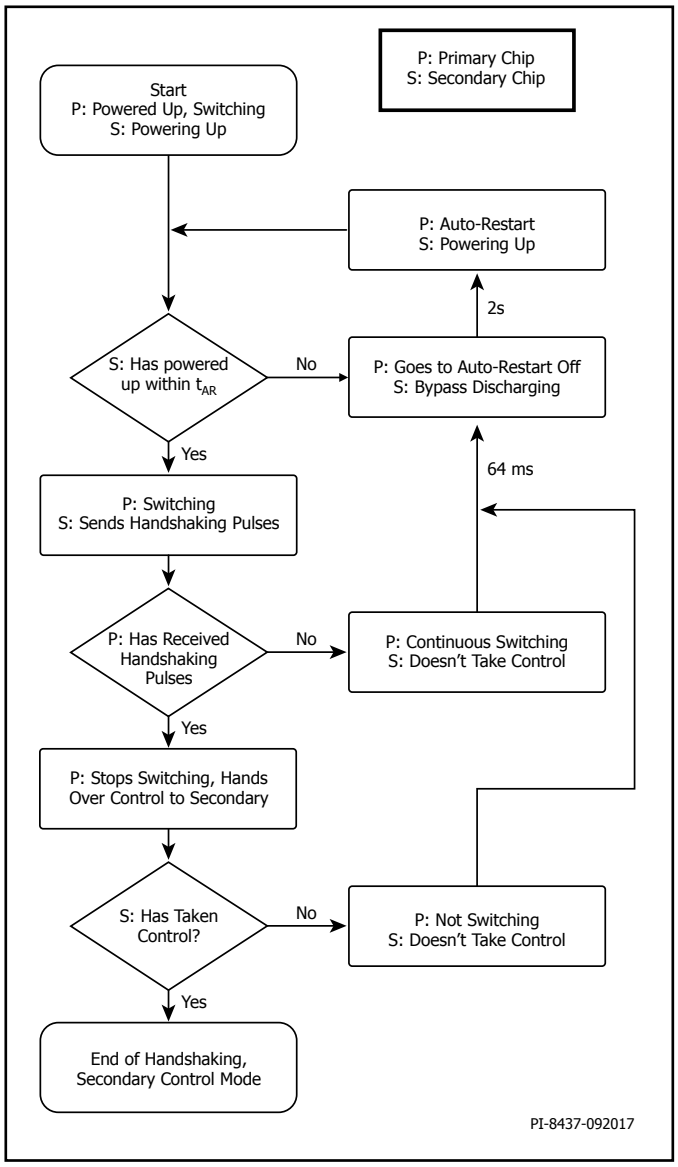


Figure 7. Primary-Secondary Handshake Flow Chart.

Wait and Listen

When the primary resumes switching after initial power-up recovery from input line voltage fault or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by 30 µs, the primary will enter secondary control and begins switching in slave mode. If no such pulses occur during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Audible Noise Reduction Engine
The LYTSwitch-6 features and active audible noise reduction mode wherein the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate - increasing noise amplitude) between 7 kHz and 12 kHz – 142 µs and 83 µs. If a secondary controller request occur within this window from the last conduction cycle, the gate drive of the power MOSFET is inhibited.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered through regulator 4.4 V (V_{BPS}) by either VOUT or FW. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SF FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SF FET in discontinuous mode operation. This is when the voltage across the $R_{DS(ON)}$ of the SR FET drops below zero volts.

In continuous conduction mode (CCM) the SR FET is turned off when the feedback pulse is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of the any overlap for the FET turn-off.

The mid-point of an external resistor divider network between the OUTPUT VOLTAGE and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is V_{REF} (1.265 V).

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins to regulate the output current in constant current regulator mode.

Minimum Off-Time
The secondary controller initiates cycle request using the inductive connection to the primary. The maximum frequency of the secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after the primary conduction to deliver energy to the load.

Maximum Switching Frequency
The maximum switch request frequency of the secondary controller is f_{SREQ}.

Frequency Soft-Start
At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

The secondary controller temporarily inhibits the FEEDBACK short protection threshold ($V_{FB(OFF)}$) until the end of the soft-start ($t_{SS(RAMP)}$) timer. After hand-shake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the $t_{SS(RAMP)}$ time period.

In the event of a short-circuit or overload at start-up, the device will regulate directly into CC (constant-current mode). The device will go into auto-restart (AR), if the output voltage does not rise above the $V_{O(AR)}$ threshold before the expiration of the soft start timer ($t_{SS(RAMP)}$) after handshake has occurred.

The secondary controller enables the FEEDBACK pin short protection mode ($V_{FB(OFF)}$) at the end of the $t_{SS(RAMP)}$ time period. If the output short maintains the FEEDBACK pin to be below short-circuit threshold the secondary will stop requesting pulses to trigger an auto-restart cycle.

If output voltage reaches regulation within the $t_{SS(RAMP)}$ time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant detection programming has already occurred.

Maximum Secondary Inhibit Period
Secondary-cycle requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

Thermal Foldback
When the secondary controller die temperature reaches 124 °C, the output power is reduced by reducing the constant current reference threshold (see Figure 8).

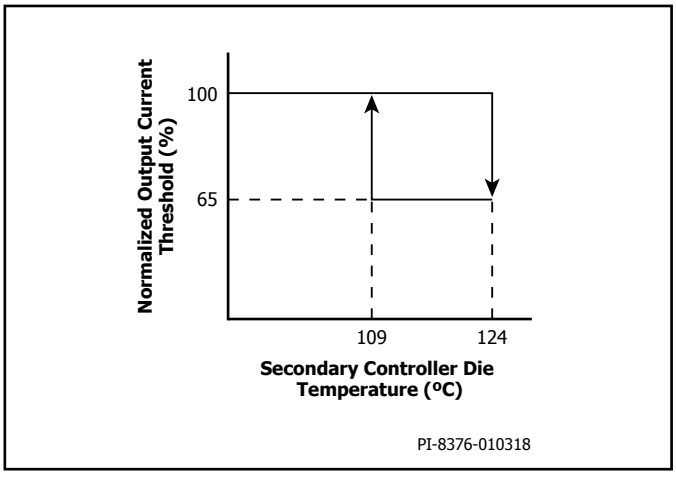


Figure 8 Normalized Primary Current vs. Secondary die Template.

Output Voltage Protection
In the event the sensed voltage on the FEEDBACK pin is 2% higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). This bleed current increases to ~200 mA in the event the FEEDBACK pin voltage is raised to beyond ~10% (strong bleed) of the internal FEEDBACK pin reference voltage. The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage for momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

If the voltage on the FEEDBACK pin is sensed to be 20% higher than the regulation threshold, a command is sent to the primary to begin an auto-restart sequence. This integrated V_{OUT} OVP can be used independently from the primary sensed OVP or in conjunction.

FEEDBACK Pin Short Detection
If the sensed FEEDBACK pin voltage is below $V_{FB(OFF)}$ at start-up, the secondary controller will complete the handshake to take control of the primary complete $t_{SS(RAMP)}$ and will stop requesting cycles to initiate auto-restart (no cycle requests made to primary for longer than $t_{AR(SK)}$ second triggers auto-restart).

During normal operation, the secondary will stop requesting pulses from the primary to initiate an auto-restart cycle when the FEEDBACK pin voltage falls below $V_{FB(OFF)}$ threshold. The deglitch filter on the protection mode is less than 10 µs. By this mechanism, the secondary will relinquish control after detecting the FEEDBACK pin is shorted to ground.

Auto-Restart Thresholds
The OUTPUT VOLTAGE pin includes a comparator to detect when the output voltage falls below $V_{VO(AR)}$ of V_{VO}, for a duration exceeding $t_{VOUT(AR)}$. The secondary controller will relinquish control when this fault condition is sensed. This threshold is meant to limit the range of constant current (CC) operation.

SECONDARY BYPASS Overvoltage Protection
The LYTSwitch-6 secondary controller features SECONDARY BYPASS pin OV feature similar to PRIMARY BYPASS pin OV feature. When the secondary is in control: in the event the SECONDARY BYPASS pin current exceeds $I_{BPS(SD)}$ (~7 mA) the secondary will send a command to the primary to initiate an auto-restart off-time ($t_{AR(OFF)}$) event.

Output Constant Current
The LYTSwitch-6 regulates the output current through an external current sense resistor between the ISENSE and SECONDARY GROUND pins where the voltage generated across the resistor is compared to internal of $I_{SV(TH)}$ (~35 mV). If constant current regulation is not required, the ISENSE pin must be tied to SECONDARY GROUND pin.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and discharge any voltage accumulation on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
The secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external MOSFET to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault. At start-up the controller will sink a current from the SYNCHRONOUS RECTIFIER DRIVE pin; an internal threshold will correlate to a capacitance of 100 pF. If the capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF (the resulting voltage is below the reference voltage), the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected to be above 100 pF (the resulting voltage is above the reference voltage), the controller will assume an SR FET is populated.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses to the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

Intelligent Quasi-Resonant Mode Switching
In order to improve conversion efficiency and reduce switching losses, the LYTSwitch-6 features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation automatically engages in DCM and disabled once the converter moves to continuous-conduction mode (CCM).

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary request to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power MOSFET.

Quasi-Resonant (QR) mode is enabled for 20 µsec after DCM is detected or ring amplitude (pk-pk) >2 V. Afterward QR switching is disabled, at which point switching may occur at any time a secondary request is initiated.

The secondary controller includes blanking of ~1 µs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground.

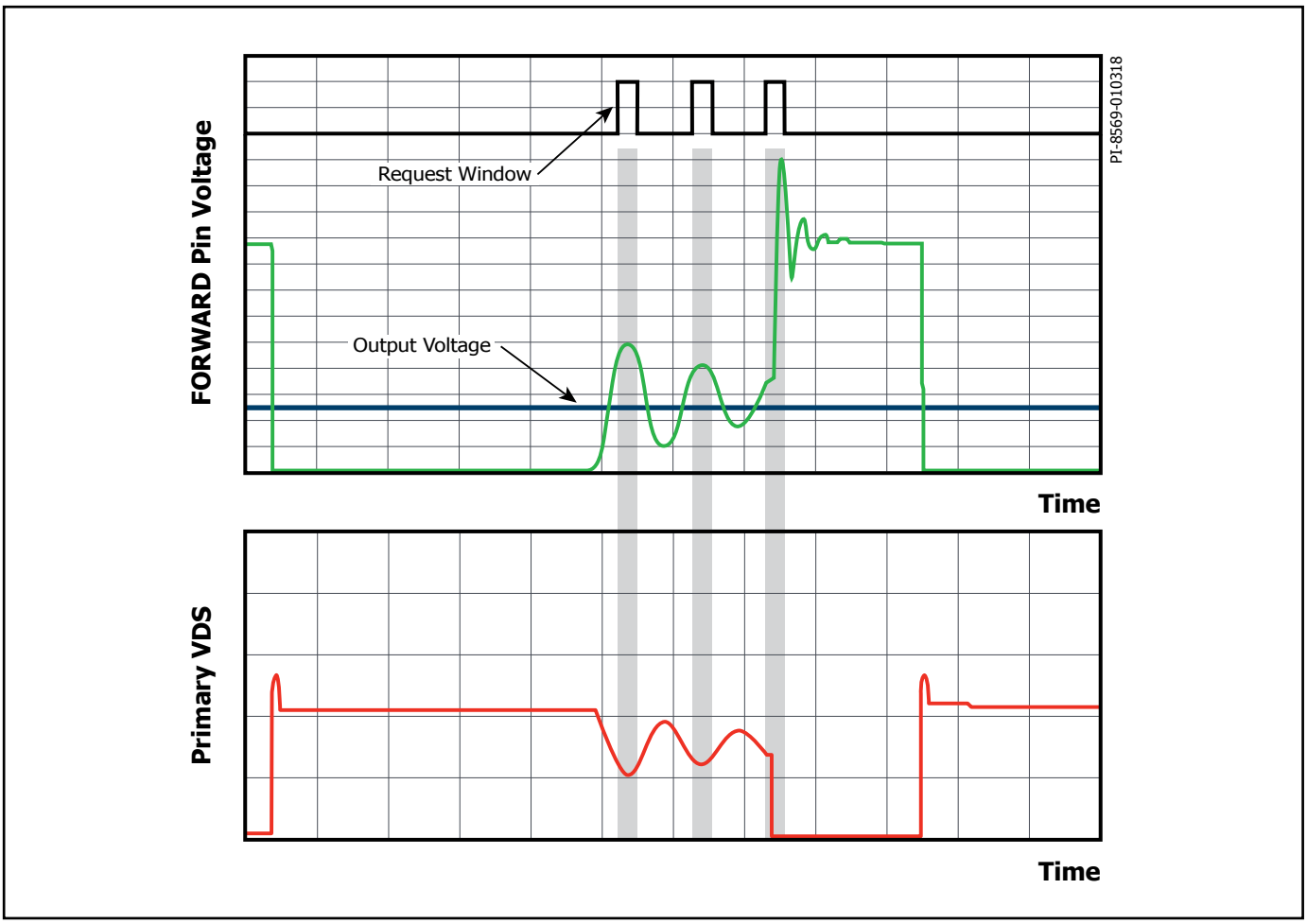


Figure 9. Intelligent Quasi-Resonant Mode Switching.

Application Example

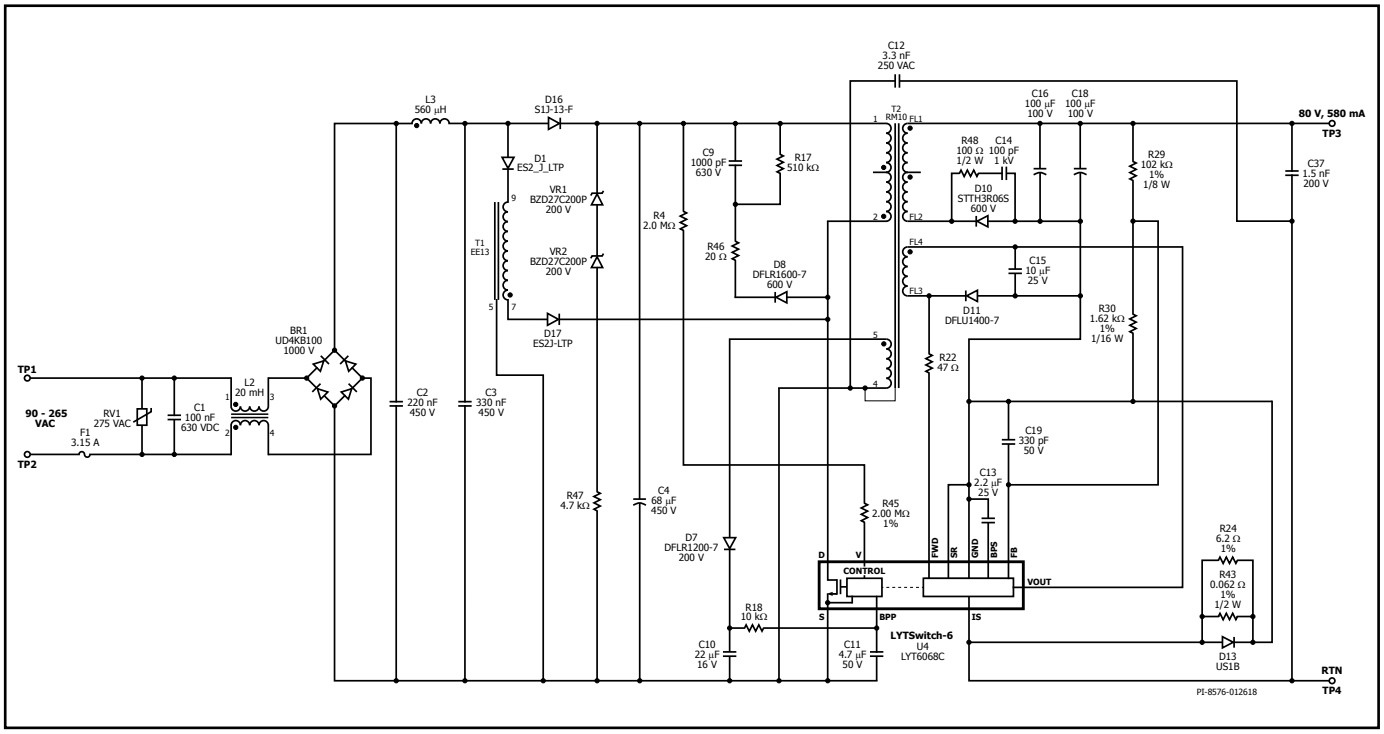


Figure 10. Schematic DER-657, 46.4 W, 80 V, 0.58 A for Universal External LED Driver Application.

The circuit shown on Figure 10 is a 45 W isolated flyback power supply with a single stage power factor correction circuit for LED lighting application. It is designed to provide a constant voltage supply of 80 V with tight voltage regulation up to 580 mA output current typically for applications where a post regulator is used for multi-LED string design such as RGBW smart lighting. And for typical single-LED string application it provides a constant output current with accurate regulation and no line-induced ripple of 580 mA from 80 V to 20 V output. The circuit is optimized to operate with high efficiency and accurate line and load regulation across an input voltage range of 90 to 265 VAC, with greater than 0.9 PF and less than 20% A-THD at 230 VAC.

Input Stage

Fuse F1 provides open-circuit protection which isolates the circuit from the input line for any catastrophic component failures. Varistor RV1 clamps any voltage spike to a safe level to protect the circuit connected after the fuse from damage due to overvoltage caused by a line transient or surge. Bridge diode BR1 rectifies the AC line voltage to provide a full-wave rectified DC voltage across the input film capacitors C2 and C3. The circuit employed a 2-stage LC EMI filter comprises of C1, L2, C2, L3, and C3 to suppress differential and common mode noise generated from the PFC and flyback switching operation.

Primary Flyback Stage

The bulk capacitor C4 filters the line ripple voltage and provides energy storage to supply DC voltage to the flyback DC-DC stage, where one end of transformer (T2) primary winding is connected to the positive terminal of the bulk capacitor (C4) while the other side is connected to the DRAIN pin of the integrated 650 V power MOSFET of LYTSwitch-6 IC (U1). Capacitor C4 also filters differential current which reduces conducted EMI noise. A low-cost RCD primary clamp comprises D8, R46, R17 and C9 limits the voltage spike caused by the transformer leakage inductance across the DRAIN and SOURCE pins of the internal MOSFET of the LYTSwitch-6 IC. The RCD primary clamp also reduces radiated and conducted EMI.

The voltage across the bulk capacitor (C4) is sensed and converted into current through INPUT VOLTAGE pin resistor (R4 and R45) to provide detection of line overvoltage. The OV pin line overvoltage threshold (I_{OV-}) determines the input overvoltage threshold.

The LYTSwitch-6 IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C11) when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T2. The value of the BPP capacitor C11 used is 4.70 µF for increased current limit. Output of the auxiliary (or bias) winding is rectified using diode D7 and filtered using capacitor C10. Resistor R18 limits the current being supplied to the BPP pin.

Power Factor Correction Stage

Power factor circuit comprises of inductor (T1) in series with blocking diode (D1 and D17) is connected to the DRAIN pin of the LYTSwitch-6 IC. High power factor correction is achieved using Switched Valley-Fill Single Stage PFC (SVF S^2PFC) configuration operating in discontinuous conduction mode (DCM). The DCM switched current from inductor T1 shapes the input current in a quasi-sinusoid waveform when the rectified voltage on C3 is less than the DC voltage on C4, which gives high power factor for line input current.

During MOSFET on-time, energy is being stored in the PFC inductor (T1) and flyback inductor (T2). During MOSFET off-time, the energy from both the PFC and flyback inductors is transferred to the secondary-side through the flyback transformer T2.

Diode D16 isolates C3 rectified AC input from C4, also provides current path for the charging of the bulk capacitor C4 especially at low line which improves efficiency. Free-wheel diodes D1 and D17 provides path for the energy stored in the PFC inductor that is transferred to the secondary-side during MOSFET turn-off time. D1 and D17 are connected in series to withstand the voltage resonance ring from the PFC inductor when the MOSFET turns off.

During no-load or light load condition (i.e. <10% load) the energy stored in the PFC inductor is more than what the secondary load requires, the excess energy from the PFC inductor is recycled to the bulk capacitor C4 which boosts up the voltage level. Zener-resistor clamp, VR1 and VR2 in series with R47 that is connected across the bulk capacitor C4 were employed to limit the voltage from rising above C4 voltage rating. The Zener clamp voltage should be less than or equal to the 450 V maximum voltage rating of bulk capacitor C4. In the event of line voltage surge or transient, in order to protect the internal mosfet of the IC from Drain overvoltage, the line over-voltage shutdown of the IC through the INPUT OVERVOLTAGE pin resistor (R5 and R45) was set to trigger at around 460 V.

Secondary Stage

The secondary-side control of the LYTSwitch-6 IC provides constant output voltage and constant output current. The secondary of the transformer is rectified by D10 and filtered by the output capacitors C16 and C18. Adding an RC snubber (R48 and C14) across the output diode reduces voltage stress across it. The SYNCHRONOUS RECTIFIER DRIVE pin is connected to the SECONDARY GROUND pin to allow the use of a cheaper ultrafast output diode instead of using an SR FET.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage via FORWARD pin or the output voltage via OUTPUT VOLTAGE pin. Capacitor C13 connected to the SECONDARY BYPASS pin of LYTSwitch-6 IC (U1) provides decoupling for the internal circuitry. In this design, the secondary-side of the IC has to be powered from a lower voltage auxiliary supply (winding FL3 and FL4) within the maximum voltage rating of the OUTPUT VOLTAGE pin, consequently the FORWARD pin has to be connected from the same output for good regulation and efficiency. The auxiliary supply is rectified and filtered by D11 and C15 respectively.

During constant voltage operation, the output voltage regulation is achieved through sensing the output voltage via network divider resistors R29 and R30. The voltage across R30 is monitored at the FEEDBACK pin and compared to an internal reference voltage threshold of 1.265 V to maintain tight regulation. Bypass capacitor C19 is placed across placed across FEEDBACK and SECONDARY GROUND pins to filter high frequency noise that may couple to the feedback signal and cause unwanted behavior such as pulse grouping.

During constant current operation, the maximum output current is set by the sense resistors R43 and R49 , the voltage across the sense resistor is compared to the ISENSE pin's internal reference threshold of 35 mV to maintain constant current regulation. Diode D13 in parallel with the current sense resistors clamps the voltage across the ISENSE and SECONDARY GROUND pin and bypasses the high current surge from the output capacitor during output short circuit conditions, thus preventing the current sense resistors from damage.

Key Applications Design Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, 220 V or higher for 230 VAC input or 115 VAC with a voltage-doubler. Input capacitor voltage should be sized to meet these criteria for AC input designs.
2. Efficiency assumptions depend on power level. Smallest device power level assumes efficiency >84% increasing to >89% for the largest device.
3. Transformer primary inductance tolerance of ±10%.
4. Reflected output voltage (VOR) is set to maintain KP = 0.8 at minimum input voltage for universal line and KP = 1 for high input line designs.
5. Maximum conduction loss for adapters is limited to 0.6 W, 0.8 W for open frame designs.
6. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 110 °C.
8. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.
9. Below a value of 1, KP is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient KP limit of ≥0.6 is recommended. This prevents the initial current limit (IINT) from being exceeded at MOSFET turn-on.
10. It is unique feature in LYTSwitch-6 device that a designer can set the operating switching frequency between 25 kHz to 95 kHz depending on the transformer design. One of the ways to effectively lower device temperature is to design the transformer to operate at low switching frequency; a good starting point is 50 kHz.

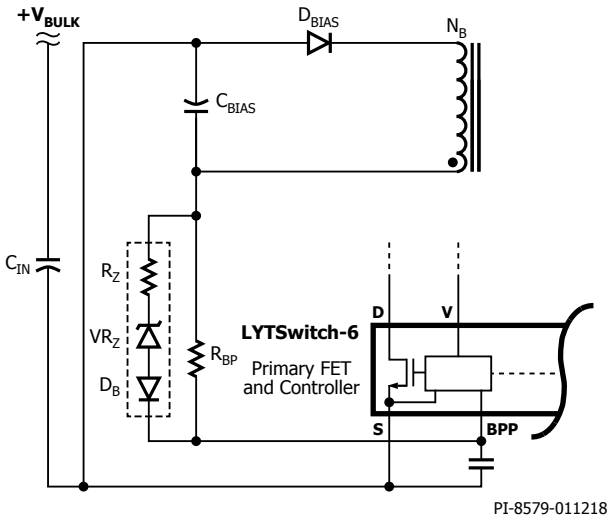
Primary-Side Overvoltage Protection

Primary-side output overvoltage protection provided by the LYTSwitch-6 IC uses an internal latch that is triggered by a threshold current of I_{SD} into the PRIMARY BYPASS pin. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

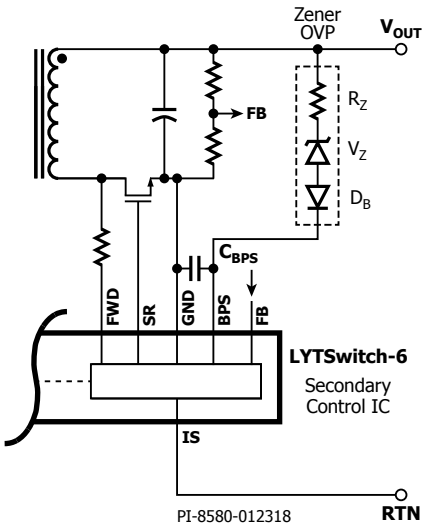
The primary sensed OVP function can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin (see Figure 11-a). The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) dependent on the coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be ideally done at the lowest input voltage and with highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be selected. A forward voltage drop of 1 V can be assumed for the blocking diode. A small signal standard recovery diode is recommended. The blocking diode prevents any reverse current charging the bias capacitor during start-up. Finally, the value of the series resistor required can be calculated such that a current higher than I_{SD} will flow into the PRIMARY BYPASS pin during an output overvoltage event.

Secondary-Side Overvoltage Protection

The secondary-side output overvoltage protection provided by the LYTSwitch-6 IC uses an internal auto-restart circuit that is triggered by an input current exceeding a threshold of $I_{BPS(SD)}$ into the SECONDARY BYPASS pin. The direct output sensed OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the



a. Primary-side OVP with High Current Pushed into BPP via Zener V_z.



b. Secondary-side OVP with High Current Pushed into BPS via Zener V_z and Resistor R_z.

Figure 11. Output Overvoltage Protection Circuits.

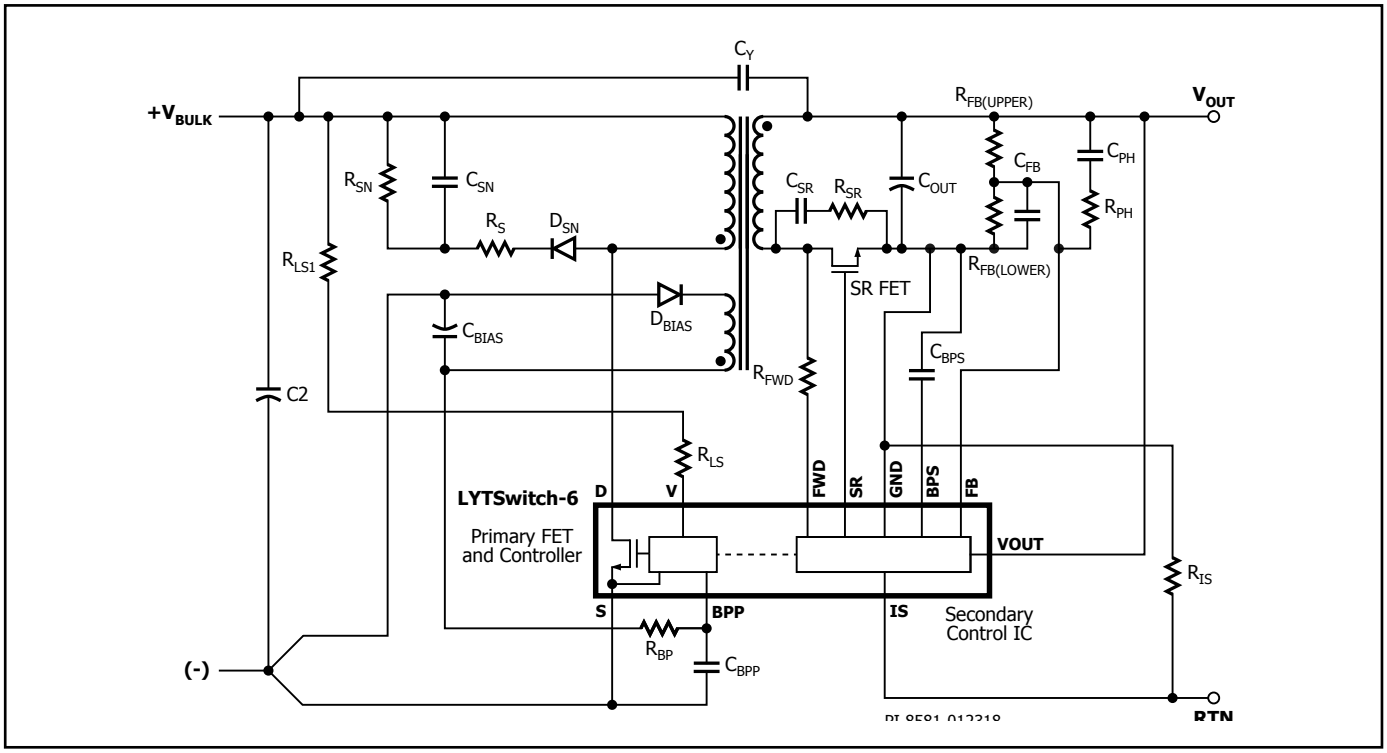


Figure 12. Typical Schematic of LYTSwitch-6 Flyback Power Supply (DC-DC Stage)

difference between 1.25 times V_{OUT} and 4.4 V minus the SECONDARY BYPASS pin voltage. It is necessary to add a low value resistor, in series with the OVP Zener diode to limit the maximum current into the SECONDARY BYPASS pin (see Figure 18-b).

Critical External Components Selection

The schematic in Figure 12 shows the most essential external components required in order for the single output LYTSwitch-6 power supply to work. The criteria of selection of some of the essential components are as follows:

Primary-Side Components of LYTSwitch-6

Primary Bypass Pin Capacitor (C_{BPP})
This capacitor works as a supply decoupling capacitor for the internal primary-side controller and also determines current limit for the internal MOSFET, that is a 4.7 µF or 0.47 µF capacitor will select INCREASED or STANDARD current limit respectively. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. A Surface mount multi-layer ceramic X7R capacitor rated for 25 V is recommended.

Line Overvoltage/Brown-In Sense Resistor (R_{LS})
Both line overvoltage and brown-in voltage are sensed by the INPUT VOLTAGE pin of the LYTSwitch-6 IC. The current from the DC input bus via R_{LS} resistor is monitored and compared to an internal current threshold.

Typical value range for R_{LS} is around 3.8 MΩ to 4 MΩ. R_{LS} is approximately equals to $V_{LOV} \times 1.414 / I_{OV-}$.

V_{LOV} is the input line overvoltage at which the power supply will instantaneously stop switching once the overvoltage threshold (I_{OV-}) is exceeded, then re-enable switching as soon as line overvoltage hysteresis ($I_{OV(H)}$) is reached. Line OV (V_{LOV}) is approximately equals $I_{OV-} \times R_{LS} / 1.414$.

The power supply will turn on once the brown-in threshold (I_{UV+}) is exceeded. Brown-in voltage is approximately equals I_{UV+} x R_{LS} / 1.414.

External Bias Supply Components (D_{BIAS}, C_{BIAS}, R_{BP})
The LYTSwitch-6 IC has an internal primary bypass regulator from the DRAIN pin to the PRIMARY BYPASS pin. This internal regulator is active during MOSFET off-time period to keep the PRIMARY BYPASS pin voltage from dropping below 5 V for the IC to operate normally especially during start-up time. Initially at start-up, the IC is powered from the internal regulator, then it will draw power from the external bias supply via the auxiliary winding as soon as the output voltage have risen high enough eventually replacing the internal regulator, hence the IC consumption will reduce, as it will be supplied from a much lower voltage as opposed to a high-voltage from the Drain. If the coupling between the bias winding and secondary winding is poor, the bias supply voltage may can drop significantly low during no-load condition that it may not be able to supply current to the PRIMARY BYPASS pin to keep the internal regulator off, if this happens then no-load input consumption will go up, therefore it is recommended to set the bias voltage to 12 V maximum, higher voltage may increase no-load input power as well. There is a trade-off between using a standard recovery diode and fast signal diode for the bias winding rectifier diode, D_{BIAS}. The former would tend to give lower radiated emi and the later lower no load input power. Since LYTSwitch-6 ICs inherently provides low input power, it is recommended to use a standard recovery diode for bias supply rectification.

A 22 µF, 50 V low ESR electrolytic aluminum capacitor is recommended for the bias supply filter, C_{BIAS}. Low ESR electrolytic capacitor reduces no-load input power. Use of ceramic surface-mount capacitor is not recommended as it may cause audible noise due to piezoelectric effect due to its mechanical structure.

To have the minimum no-load input power and high full load power efficiency, Resistor R_{BP} in Figure 12 should be selected such that the current through this resistor should be higher than the PRIMARY BYPASS pin supply current.

The PRIMARY BYPASS pin supply current at operating switching frequency can be calculated as shown in the following equation;

$$I_{SSW} = \left(\frac{F_{SW}}{132\,K}\right) \times (Is2 - Is1) + Is1$$

Where;
I_{SSW}: PRIMARY BYPASS pin supply current at operating switching frequency
F_{SW}: operating switching frequency (kHz)
I_{S1}: PRIMARY BYPASS pin supply current at no switching (refer to data sheet)
I_{S2}: PRIMARY BYPASS pin supply current at 132 kHz (refer to data sheet)

The primary bypass voltage will be around 5.3 V if bias current is higher than PRIMARY BYPASS pin supply current. If primary bypass voltage is around 5.0 V, then this indicates that the current through R_{BP} is less than the PRIMARY BYPASS pin supply current and the current from the DRAIN pin. Ensure that the voltage at the PRIMARY BYPASS pin never fall below 5.0 V except during start-up time.

To determine maximum value of R_{BP};

$$R_{BP}[V_{BIAS(NO-LOAD)} - V_{BPP}]/I_{SSW;} V_{BPP} = 5.3\,V$$

Primary Clamp Network Across Primary Winding (D_{SN}, R_S, R_{SN}, and C_{SN})
Figure 14, R2CD clamp is the most commonly used clamp in most low power supplies due to cost advantage. For higher power supply designs, the Zener clamp or the R2CD plus Zener clamp can be used to achieve better efficiency. It is advisable to limit the peak Drain voltage to 90% of BV_{DSS} under worst-case conditions such as maximum input voltage, maximum overload power or output short-circuit. In Figure 13, the clamp diode, D_{SN} must be a standard recovery glass passivated type or a fast recovery type with a reverse recovery time of less than 500 ns. Use of standard recovery glass passivated diodes results in recovery of some of the clamp energy in each cycle and helps in improving average efficiency. The diode conducts momentarily each time the MOSFET inside LYTSwitch-6 IC turns off and energy from the leakage reactance is transferred to the clamp capacitor C_{SN}. Resistor R_S, which is in the series path, offers damping and prevents excessive ringing due to resonance between the leakage reactance and the clamp capacitor C_{SN}. Resistor RS_N bleeds off the energy stored inside the capacitor C_{SN}. Supplies using different LYTSwitch-6 devices in the family will have different peak primary current, leakage inductances and therefore leakage energy. Capacitor C_{SN}, R_{SN} and R_S will therefore be optimized for each design. As a general rule minimize the value of capacitor C_{SN} and maximize the value of resistor R_{SN} and R_S, while still meeting 90% of BV_{DSS} limit recommended for operation at highest input voltage and full load. The value of R_S should be large enough to dampen the ring on the required time, but must not be too large to cause the drain voltage to exceed 90% of BV_{DSS}. A ceramic capacitor that uses dielectric, such as Z5U when used in clamp circuit for C_{SN} may generate audio noise, so a polyester film type may be used.

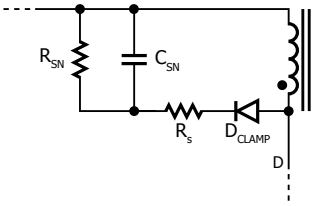
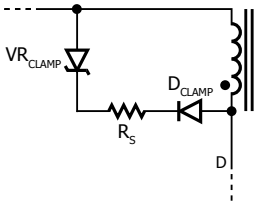
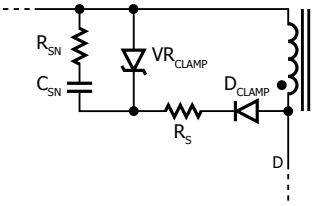
Common Primary Clamp Configurations		
R2CD	**R2CD (Zener Clamp)**	**R2CD + Zener**
		

Figure 13. Recommended Primary Clamp Components.

Primary Clamp Circuit			
Benefits	**RCD**	**Zener**	**RCD + Zener**
Component Cost	Low	Medium	High
No-Load Input Power	High	Low	Medium
Light-Load Efficiency	Low	High	Medium
EMI Suppression	High	Low	Medium

Table 2. Benefits of Primary Clamp Circuits.

Secondary-Side Components of f LYTSwitch-6

Secondary Bypass Pin Capacitor (C_{BPS})

This capacitor works as a supply decoupling capacitor for the internal secondary-side controller. A surface-mount, 2.2 µF, 25 V, multi-layer ceramic capacitor is recommended for satisfactory operation of the IC. Since the SECONDARY BYPASS pin voltage needs to reach 4.4 V earlier than output voltage reaches to the regulation voltage level, the significantly higher secondary bypass capacitor value will lead to output voltage overshoot during start-up. The values lower than 1.5 µF may not be enough capacitance, which can cause unpredictable operation. The capacitor must be located adjacent to the IC pins. The 25 V rating is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops with applied voltage. 10 V rated capacitors are not recommended for this reason. Capacitors with X5R or X7R dielectrics should be used for best results.

FORWARD Pin Resistor (R_{FWD})

The FORWARD pin is connected to the Drain terminal of the synchronous rectifier MOSFET (SR FET). This pin is used to sense the Drain voltage of the SR FET to precisely turn-on and turn-off. This pin is also used to provide charge to the SECONDARY BYPASS pin capacitance whenever output voltage is lower than the secondary bypass voltage. A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current and works for very wide range of output voltages. A higher or lower resistor value should not be used as it can affect device operation such as the timing of the synchronous rectifier drive. Care should be taken to ensure that the voltage at the FORWARD pin never exceeds its absolute maximum voltage. If in any design, the FORWARD pin voltage exceeds the FORWARD pin absolute maximum voltage, the IC will be damaged.

FEEDBACK Pin Divider Network ($R_{FB(UPPER)}$, $R_{FB(LOWER)}$)

A suitable resistor voltage divider should be connected from the output of the power supply to the FEEDBACK pin of the LYTSwitch-6 IC such that for the desired output voltage, the voltage at the FEEDBACK pin will be 1.265 V. A decoupling capacitor (C_{FB}) of 330 pF is recommended to be connected from the FEEDBACK pin to SECONDARY GROUND pin and serves as a decoupling capacitor for the FEEDBACK pin to prevent switching noise from affecting operation of the IC.

SR MOSFET Operation and Selection

Although a simple diode rectifier and filter works for the output, use of a SR FET enables the significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the LYTSwitch-6 IC (no additional resistors should be connected in the gate circuit of the SR FET). The SR FET is turned off once the V_{DS} of the SR FET reaches 0 V. A FET with 18 mW $R_{DS(ON)}$ is appropriate for a 5 V, 2 A output, and a FET with 8 mW $R_{DS(ON)}$ is suitable for designs rated with a 12 V, 3 A output. The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A FET with a high threshold voltage is therefore not suitable; FETs with a threshold voltage of 1.5 V to 2.5 V are ideal although MOSFETs with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets specify $R_{DS(ON)}$ across temperature for a gate voltage of 4.5 V.

There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the LYTSwitch-6 IC detects end of the flyback cycle, voltage across SR FET $R_{DS(ON)}$ reaches 0 V, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. Use of the Schottky diode parallel to the SR FET may be added to provide higher efficiency and typically a 1 A surface mount Schottky diode is adequate. However the gains are modest, for a 5 V, 2 A design the external diode adds ~0.1% to full load efficiency at 85 VAC and ~0.2% at 230 VAC.

The voltage rating of the Schottky diode and the SR FET should be at least 1.3 to 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. 60 V rated FETs and diodes are suitable for most 5 V designs that use a VOR <60 V, and 100 V rated FETs and diodes are suitable for 12 V designs.

The interaction between the leakage reactance of the output windings and the SR FET capacitance (COSS) leads to ringing on the voltage waveform at the instance of voltage reversal at the winding due to primary MOSFET turn-on. This ringing can be suppressed using a RC snubber connected across the SR FET. A snubber resistor in the range of 10 W to 47 W may be used (higher resistance values lead to noticeable drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs.

Output Filter Capacitance (C_{OUT})
Low ESR and high RMS ripple current rating aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies for ballast applications. Typically, 300 µF to 400 µF of aluminum-electrolytic capacitance per ampere of output current is adequate. The other factor that influences choice of the capacitance is the output ripple. Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin be used.

Output Current Sense Resistor (R_{IS})
For output constant current (CC) operation, external current sense resistor R_{IS} should be connected between this ISENSE pin and the SECONDARY GROUND pin of the IC as shown in Figure 14. If constant current (CC) regulation is not required, this pin should be connected to the SECONDARY GROUND pin of the IC.

The voltage generated across the resistor is compared to an internal reference Current Limit Voltage Threshold ($I_{SV(TH)}$) of approximately 35 mV.

Hence, the external current sense resistor R_{IS} can be approximated with equation;

$$R_{IS} = IOUT_{CC} / I_{SV(TH)}$$

The placement of the R_{IS} resistor must be close to ISENSE and SECONDARY GROUND pin with short traces in order to avoid ground impedance noise that may cause instability especially in constant current operation.

Output Post Filter Components (L_{PF}, C_{PF})
If necessary a post filter (L_{PF} and C_{PF}) can be added to reduce high frequency switching noise and ripple. Inductor L_{PF} should be in the range of 1 µH – 3.3 µH with a current rating above the peak output current. Capacitor C_{PF} should be in the range of 100 µF to 330 µF with a voltage rating ≥ 1.25 × V_{OUT}. If a post filter is used then the output voltage sense resistor should be connected before the post filter inductor.

Recommendations for Circuit Board Layout

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pin. See Figure 14.

Bypass Capacitors
The PRIMARY BYPASS (C_{BPP}), SECONDARY BYPASS (C_{BPS}) pin and feedback decoupling capacitors must be located directly adjacent to the PRIMARY BYPASS - SOURCE, SECONDARY BYPASS - SECONDARY GROUND and FEEDBACK - SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Signal Components
External components R_{LS}, R_{BP}, $R_{FB(UPPER)}$, $R_{FB(LOWER)}$ and R_{IS} which are used for monitoring feedback information must be placed as close as possible to the IC pin with short trace.

Critical Loop Area
Circuits where high dv/dt or di/dt occurs should be kept as small and as tight as possible. The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible. Ideally, no loop area should be placed inside another loop area as shown in Figure 14. This will minimize cross-talk between circuits.

Primary Clamp Circuit
A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and IC.

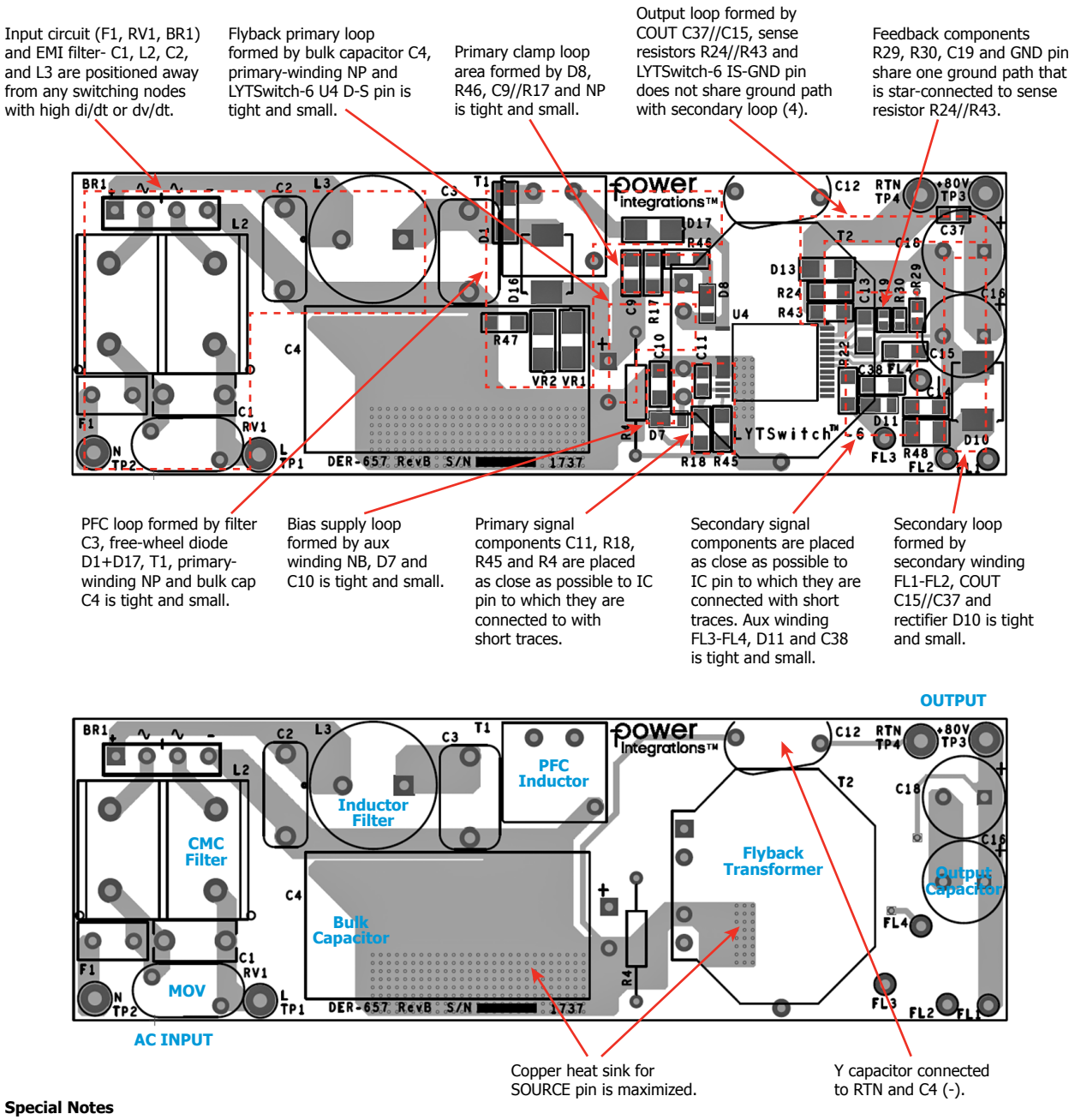
Y Capacitor
The placement of the Y capacitor should be directly from the primary input filter capacitor positive terminal to the output positive or return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the IC. Note that if an input pi EMI filter (C1, LF and C2) is used, then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output Rectifier Diode
For best performance, the area of the loop connecting the secondary winding, the output rectifier diode, and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the terminals of the rectifier diode for heat sinking.

ESD Immunity
Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD or hi-pot requirements. The spark gap is best placed between output return and/or positive terminals and one of the AC inputs after the fuse. In this configuration a 6.4 mm (5.5 mm is acceptable – dependent on customer requirement) spark gap is more than sufficient to meet the creepage and clearance requirements of many applicable safety standards. This is less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input.

Drain Node
The drain switching node is the dominant noise generator. As such the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin, and trace width and length in this circuit should be minimized.

PCB Layout Example



Special Notes

- All loops are separated; no loop is inside a loop. This will avoid ground impedance noise coupling.
- Maintain trace surface area and length of high dv/dt nodes such as DRAIN, as small and short as possible to minimized RFI generation.
- No signal trace (quiet trace) such as Y capacitor and feedback return must be routed near or across noisy nodes (high dv/dt or di/dt) such as DRAIN, underneath transformer belly, switching side of any winding or output rectifier diode to avoid capactively or magnetically coupled noise.
- No signal trace must share path with traces having an AC switching current such as output capacitor. Connection must be star-connected to capacitor pad in order to avoid ground impedance coupled noise.

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Figure 14. TOP and BOTTOM Sides – Ideal Layout Example Showing Tight Loop Areas for Circuit with High dv/dt and di/dt, Component Placement.

Recommendations in Reducing No-load Consumption

The LYTSwitch-6 IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Use of a bias winding is however required to provide supply current to the PRIMARY BYPASS pin once the LYTSwitch-6 IC has started switching. An auxiliary (bias) winding provided on the transformer serves this purpose. A bias winding driver supply to the PRIMARY BYPASS pin enables design of power supplies with no-load power consumption less than 100 mW. Resistor R_{BP} shown in Figure 12 should be adjusted to achieve the lowest no-load input power.

Other areas that may help reduce further no-load consumption when optimized are the following;

1. Low value of primary clamp capacitor, C_{SN}.
2. Schottky or ultrafast diode for bias supply rectifier, D_{BIAS}.
3. Low ESR capacitor for bias supply filter capacitor, C_{BIAS}.
4. Low value SR FET RC snubber capacitor, C_{SR}.
5. Tape between primary winding layers, and multi-layer tapes between primary and secondary windings to reduce inter winding capacitance.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area. (See Figure 14)
2. A small capacitor parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. A resistor (2 – 47 Ω) in series with the bias winding helps reduce radiated EMI.
4. A small resistor and ceramic capacitor (< 22 pf) in series across primary shown in Figure 19 and/or across secondary winding (< 100 pf) may help reduce conducted and/or radiated EMI. If value is large, then it may affect no-load consumption.
5. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common mode noise. However, the same performance can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at input to improve conducted and radiated EMI margins.
6. Adjusting SR FET RC snubber component values can help reduce high frequency radiated and conducted EMI.
7. A pi filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI. A ferrite bead as shown in Figure 14 can be added to further improve emi margin with minimal cost.
8. A resistor across a differential inductor reduces the Q factor which can reduce EMI above 10 MHz. Check the low frequency EMI below 5 MHz may slightly increase.
9. A 1 μF ceramic capacitor connected at the output of the power supply may help to reduce radiated EMI.
10. Slow diode (i.e. 250 ns < t_{RR} < 500ns) on bias rectifier (D_{BIAS}) is generally good for conducted emi > 20 MHz and radiated emi > 30 MHz.

Thermal Management Considerations

The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, this area should be maximized for good heat sinking. Similarly for output SR FET, maximize the PCB area connected to the pins on the package through which heat is dissipated in the SR FET.

Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 90 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage. Further de-rating can be applied depending on any additional specific requirements.

Heat Spreader

For enclosed high power applications such as external LED ballast or similar applications with high ambient environment, using the PCB as a heat sink may not be enough for the IC to operate within specified operating temperature, therefore a metal heat spreader (material dependent on designer preference) may be necessary to manage the operating temperature of device within acceptable level.

Unless ceramic material is used as a heat sink, the safety barrier must not to be breached. The heat spreader is formed by combination of heat-spreader material (copper or aluminum), 0.4 mm mylar pad for reinforced isolation and thermally conductive pad for better heat transfer from device to heat-spreader.

As shown in Figure 15, basic idea how to implement the attachment of heat spreader to an InSOP-24D package with safety creepage consideration between primary-side and secondary-side pins of LYTSwitch-6 IC.

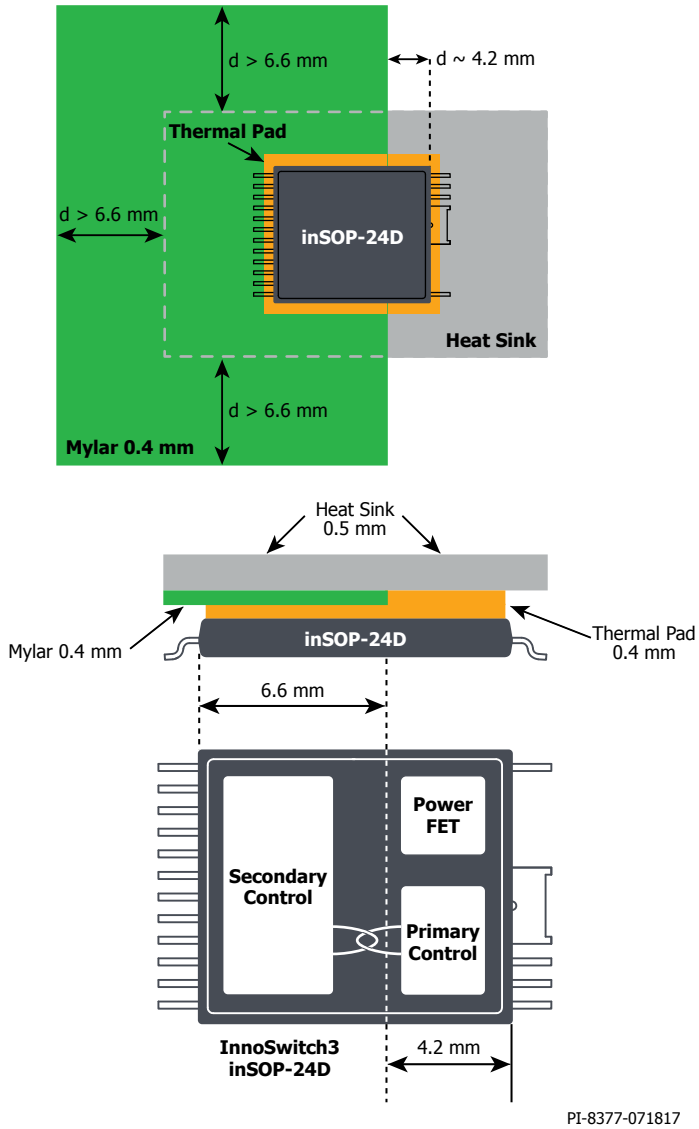


Figure 15. Simplified Diagram of Heat spreader Attachment to an InSOP-24D Package.

Recommended Position of InSOP-24D Package with Respect to Transformer

The PCB underneath the transformer and InSOP-24D must be rigid. In case of large size cores used on the board with thin PCB, i.e. <1.5 mm, it is recommended to move the transformer away from InSOP package. Cutting slot on the PCB that runs near or underneath the InSOP package is generally not recommended as this weakens the PCB. And in the case of long PCB, it is recommended to put mechanical support or post in the middle or near the InSOP package.

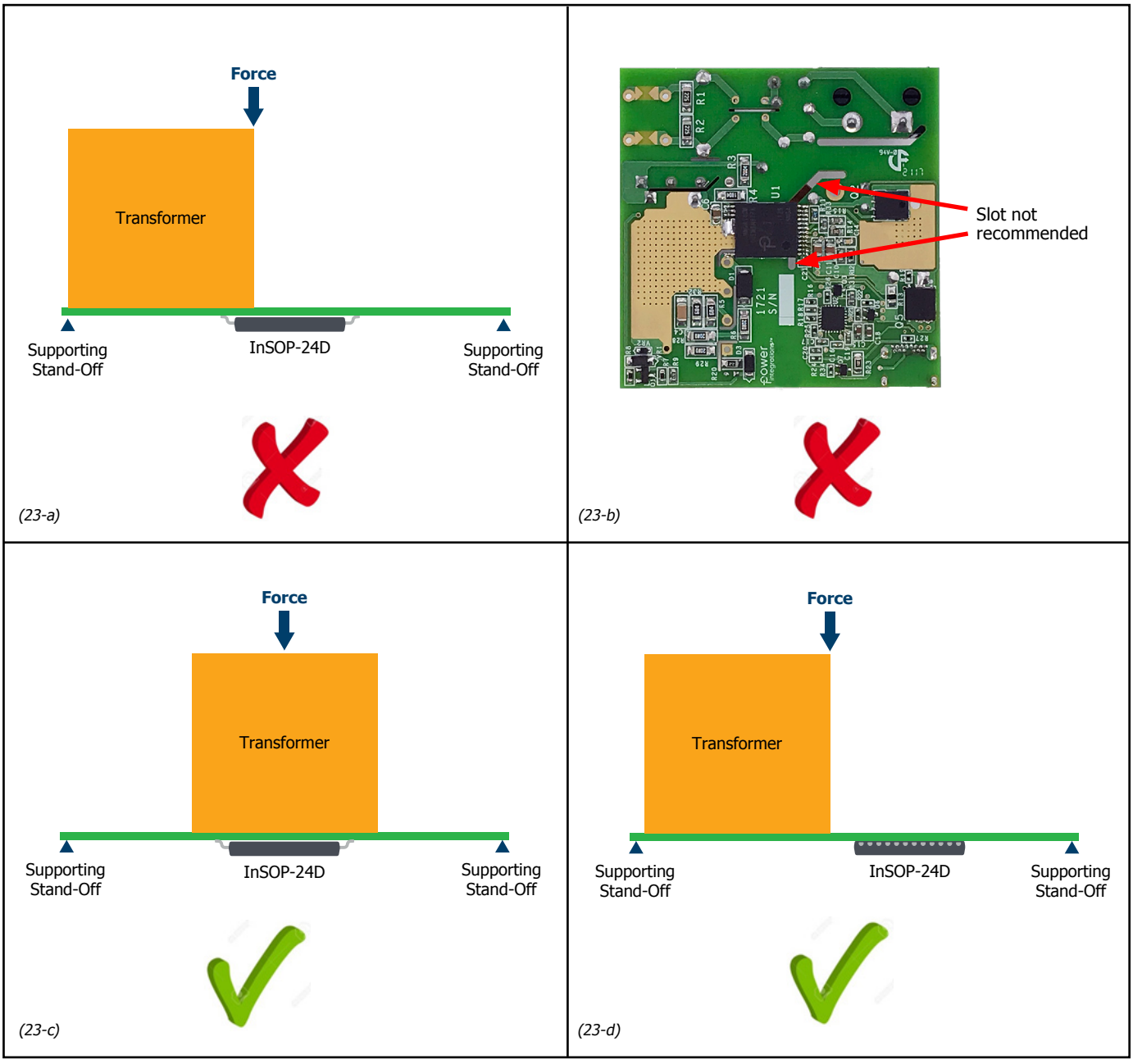


Figure 16. Recommended Position of InSOP-24D Package Shown with Check Mark.

Quick Design Checklist

As with any power supply, the operation of all LYTSwitch-6 designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions. As a minimum, the following tests are strongly recommended:

Maximum Drain Voltage – Verify that V_{DS} of LYTSwitch-6 IC and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.

Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review Drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum Drain current for the primary MOSFET should be below the specified absolute maximum ratings.

Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature. Verify that temperature specification limits for LYTSwitch-6 IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margins should be allowed for part-to-part variation of the $R_{DS(ON)}$ of the LYTSwitch-6 IC. Under low-line, maximum power, a maximum LYTSwitch-6 SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Other Applications Design Example

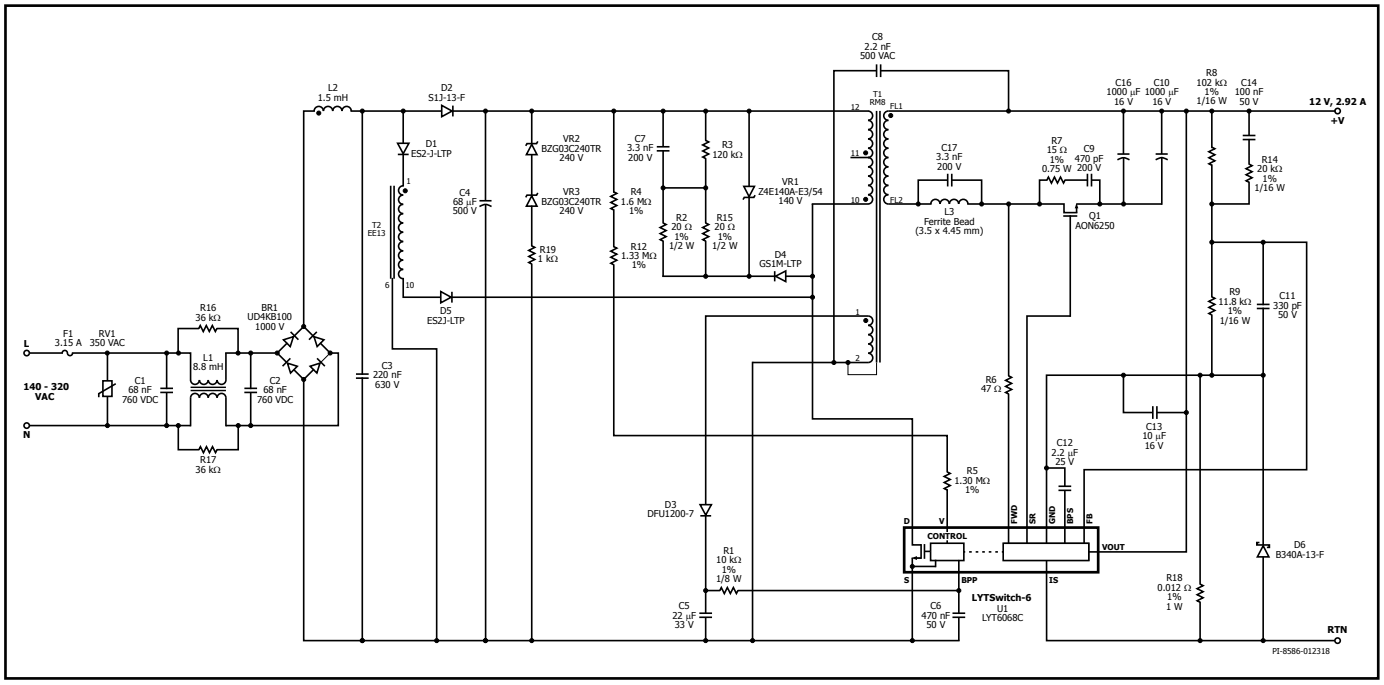


Figure 17. Schematic of DER-637, 35 W, 12 V, 2.92 A, 140 VAC – 320 VAC using LYSwitch-6 LYT6068C with Synchronous Rectification.

A High Efficiency, 35 W, 12 V with Synchronous Rectification LED Ballast – Universal Input Power Supply

The circuit shown on Figure 17 is a 35 W isolated flyback power supply with a single-stage power factor correction circuit for LED lighting application. It is designed to provide a constant voltage supply of 12 V with accurate voltage regulation up to 2.92 amperes output current typically for applications where a post regulator is used for multi-LED string design such as RGBW smart lighting. And for typical single-LED string application it provides a constant output current with tight regulation and no line-induced ripple of 2.92 amperes from 12 V to 3 V output. The circuit is optimized to operate with high efficiency and accurate line and load regulation across an input voltage range of 140 to 320 VAC, with greater than 0.9 PF and less than 20 % A-THD at 230 VAC.

Input Stage

Fuse F1 provides open-circuit protection which isolates the circuit from the input line for any catastrophic component failures. Varistor RV1 clamps any voltage spike to a safe level to protect the circuit connected after the fuse from damage due to overvoltage caused by a line transient or surge. Bridge diode BR1 rectifies the AC line voltage to provide a full-wave rectified DC voltage across the input film capacitors C3 and C4. The circuit employed a 2-stage LC EMI filter comprises of C1, L1, C2, L2, and C3 to suppress differential and common mode noise generated from the PFC and flyback switching operation.

Primary Flyback Stage

The bulk capacitor C4 filters the line ripple voltage and provides energy storage to supply DC voltage to the flyback DC-DC stage, where one end of transformer (T1) primary winding is connected to the positive terminal of the bulk capacitor (C4) while the other side is connected to the DRAIN pin of the integrated 650 V power MOSFET of LYTSwitch-6 IC (U1). Capacitor C4 also filters differential current which reduces conducted EMI noise. A low cost RCD primary clamp comprises of D4, R2//R15 and R3//C7 limits the voltage spike caused by the transformer leakage inductance across the DRAIN and SOURCE pins of the internal MOSFET of LYTSwitch-6 IC. Clamp Zener VR1 was employed to clamp the Drain voltage spike during start-up full load at 320 VAC. The RCD primary clamp also reduces radiated and conducted EMI.

The voltage across the bulk capacitor (C4) is sensed and converted into current through INPUT OVERVOLTAGE pin resistor (R4 and R12) to provide detection of line overvoltage and brown-in voltage. The overvoltage threshold (I_{OV+}) determines the input overvoltage threshold, while undervoltage brown-in threshold (I_{UV+}) determines the line turn-on voltage.

The LYTSwitch-6 IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C6) when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. The value of the PRIMARY BYPASS pin capacitor C6 used is 470 nF for standard current limit. Output of the auxiliary (or bias) winding is rectified using diode D3 and filtered using capacitor C5. Resistor R1 limits the current being supplied to the PRIMARY BYPASS pin.

Power Factor Correction Stage

Power factor circuit comprises of inductor (T2) in series with blocking diode (D1 and D5) is connected to the DRAIN pin of the LYTSwitch-6 IC. High power factor correction is achieved using Switched Valley-Fill Single Stage PFC (SVF S2PFC) configuration operating in discontinuous conduction mode (DCM). The DCM switched current from inductor T2 shapes the input current in a quasi-sinusoid waveform when the rectified voltage on C3 is less than the DC voltage on C4, which gives high power factor for line input current.

During MOSFET on-time, energy is being stored in the PFC inductor (T2) and flyback transformer (T1). During MOSFET off-time, the energy from both the PFC and flyback inductors is transferred to the secondary-side through the flyback transformer T1.

Diode D2 isolates C3 rectified AC input from C4, also provides current path for the charging of the bulk capacitor C4 especially at low-line which improves efficiency. Free-wheel diodes D1 and D5 provide path for the energy stored in the PFC inductor that is transferred to the secondary-side during MOSFET turn-off time. Diode D1 and D5 are connected in series to withstand the voltage resonance ring from the PFC inductor when the MOSFET turns off.

During no-load or light load condition (i.e. <10% load) the energy stored in the PFC inductor (T2) may be more than what the secondary load requires, the excess energy from the PFC inductor is recycled to the bulk capacitor C4 which boosts the voltage level higher. Zener-resistor clamp, VR2 and VR3 in series with R19 that is connected across the bulk capacitor C4 were employed to limit the voltage from rising above its voltage rating. The Zener clamp voltage should be less than or equal to the 500 V maximum voltage rating of bulk capacitor C4. In the event of line voltage surge or transient, in order to protect the internal MOSFET of the IC from Drain over-voltage, the line overvoltage shutdown of the IC through the INPUT VOLTAGE pin resistor (R4 and R5) was set to trigger at around 490 V.

Secondary Stage

The secondary-side control of the LYTSwitch-6 IC provides constant output voltage and constant output current. The secondary of the transformer is rectified by SR FET Q1 and filtered by the output capacitors C10 and C16. Adding a RC snubber (R7 and C9) across the SR FET reduces voltage stress across it.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage via FORWARD pin or the output voltage via OUTPUT VOLTAGE pin. Capacitor C13 connected to the SECONDARY BYPASS pin of LYTSwitch-6 IC (U1) provides decoupling for the internal circuitry.

During constant voltage operation, the output voltage regulation is achieved through sensing the output voltage via network divider resistors R8 and R9. The voltage across R9 is monitored at the FEEDBACK pin and compared to an internal reference voltage threshold of 1.265 V to maintain accurate regulation. Bypass capacitor C11 is placed across FEEDBACK and SECONDARY GROUND pins to filter high frequency noise that may couple to the feedback signal and cause unwanted behavior such as pulse grouping.

During constant current operation, the maximum output current is set by the sense resistors R18, the voltage across the sense resistor is compared to the ISENSE pin's internal reference threshold of 35 mV to maintain constant current regulation. Diode D16 parallel with the current sense resistor R18 clamps the voltage across the ISENSE and SECONDARY GROUND pin and bypasses the high current surge from the output capacitor during output short circuit condition, thus preventing the current sense resistors from damage.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage: ..... -0.3 V to 650 V / 725 V
DRAIN Pin Peak Current: LYT60x3C ..... 1.04 A (1.95 A)[3]
LYT60x5C ..... 1.84 A (3.45 A)[3]
LYT60x7C ..... 2.64 A (4.95 A)[3]
LYT60x8C ..... 2.96 A (5.55 A)[3]
BPP/BPS Pin Voltage ..... -0.3 to 6 V
BPP/BPS Current ..... 100 mA
FW Pin Voltage ..... -1.5 V to 150 V
FB Pin Voltage ..... -0.3 V to 6 V
SR Pin Voltage ..... -0.3 V to 6 V
V Pin Voltage (LYT606xC) ..... -0.3 V to 650 V
V Pin Voltage (LYT607xC) ..... -0.3 V to 725 V
VOUT Pin Voltage ..... -0.3 V to 27 V
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[4] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Lead Temperature[5] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Higher peak Drain current is allowed while the Drain voltage is simultaneously less than 400 V.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.

Thermal Resistance

Thermal Resistance:
(θ_{JA}) ..... 76 °C/W[1], 65 °C/W[2]
(θ_{JC}) ..... 8 °C/W[3]

Notes:
1. Soldered to 0.36 sq. inch (232 mm²) 2 oz. (610 g/m²) copper clad.
2. Soldered to 1 sq. inch (645 mm²), 2 oz. (610 g/m²) copper clad.
3. The case temperature is measured on the top of the package.

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24	1.5	A
Primary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (device mounted in socket)	0.125	W

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
Start-Up Switching Frequency	f_{SW}	T_J = 25 °C	22	25	27	kHz
Jitter Frequency	f_M	T_J = 25 °C, f_{SW} = 100 kHz	0.8	1.25	1.70	kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C	12.4	14.6	16.9	µs
Minimum Primary Feedback Block-Out Timer	t_{BLOCK}				$t_{OFF(MIN)}$	µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
BPP Supply Current	I_{S1}	$V_{BPP} = V_{BPP}$ + 0.1 V (MOSFET not Switching) T_J = 25 °C		145	200	425	µA
	I_{S2}	$V_{BPP} = V_{BPP}$ + 0.1 V (MOSFET Switching at f_{SW}) T_J = 25 °C	LYT6063C	0.32	0.43	0.61	mA
			LYT6065C	0.49	0.65	1.03	
			LYT6067C	0.77	1.03	1.38	
			LYT6068C	0.90	1.20	1.75	
			LYT6073C	0.36	0.48	0.65	
			LYT6075C	0.59	0.79	1.10	
			LYT6077C	0.77	1.20	1.73	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C		-1.75	-1.35	-0.88	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C		-5.98	-4.65	-3.32	
BPP Pin Voltage	V_{BPP}	T_J = 25 °C		4.65	4.9	5.15	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$			0.22	0.39	0.55	V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA		5.15	5.36	5.65	V
BPP Power-Up Reset Threshold Voltage	$V_{BPP(RESET)}$	T_J = 25 °C		2.8	3.15	3.5	V
OV Pin Line Overvoltage Threshold	I_{OV-}	T_J = 25 °C		106	115	118	µA
OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C		6	7	8	µA
OV Pin Line Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C			3		µs
UV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		23.95	26.06	28.18	µA
Line Fault Protection							
VOLTAGE Pin Voltage Rating	V_V	T_J = 25 °C		1000			V

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF	I_{LIMIT}	di/dt = xxxx mA/µs T_J = 25 °C	LYT60x3C	511	550	589	mA
		di/dt = 212.5 mA/µs T_J = 25 °C	LYT60x5C	883	950	1017	
		di/dt = 300 mA/µs T_J = 25 °C	LYT60x7C	1348	1450	1552	
		di/dt = 375 mA/µs T_J = 25 °C	LYT6068C	1534	1650	1766	
Increased Current Limit (BPP) Capacitor = 4.7 µF	$I_{LIMIT+1}$	di/dt = xxxx mA/µs T_J = 25 °C	LYT60x3C	591	650	709	mA
		di/dt = 212.5 mA/µs T_J = 25 °C	LYT60x5C	1046	1150	1254	
		di/dt = 300 mA/µs T_J = 25 °C	LYT60x7C	1501	1650	1799	
		di/dt = 375 mA/µs T_J = 25 °C	LYT6068C	1683	1850	2017	
Overload Detection Frequency	f_{OVL}	T_J = 25 °C See Note A		102	110	118	kHz
Auto-Restart On-Time	t_{AR}	T_J = 25 °C	fs = 100 kHz	75	82	89	ms
BYPASS Pin Fault Detection Threshold Current	I_{SD}	T_J = 25 °C		6.0	8.9	11.3	mA
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C		1.7		2.1	sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C		0.17	0.20	0.23	sec

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	LYT6063C $I_D = I_{LIMIT+1}$	T_J = 25 °C		4.90	5.64	Ω
			T_J = 100 °C		7.60	8.74	
		LYT6065C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	
			T_J = 100 °C		3.02	3.47	
		LYT6067C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.02	1.17	
			T_J = 100 °C		1.58	1.82	
		LYT6068C $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.86	0.99	
			T_J = 100 °C		1.33	1.53	
		LYT6073C $I_D = I_{LIMIT+1}$	T_J = 25 °C		4.42	5.08	
			T_J = 100 °C		6.85	7.88	
		LYT6075C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.95	2.24	
			T_J = 100 °C		3.02	3.47	
		LYT6077C $I_D = I_{LIMIT+1}$	T_J = 25 °C		1.20	1.38	
			T_J = 100 °C		1.86	2.14	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP} + 0.1$ V V_{DS} = 150 V T_J = 25 °C			15		µA
	I_{DSS2}	$V_{BPP} = V_{BPP} + 0.1$ V V_{DS} = 325 V T_J = 25 °C				200	µA
Breakdown Voltage	BV_{DSS}	$V_{BPP} = V_{BPP} + 0.1$ V T_J = 25 °C	LYT606xC	650			V
			LYT607xC	725			
Drain Supply Voltage				50			V
Thermal Shutdown	T_{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$				70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary						
FEEDBACK Pin Voltage	V_{FB}	T_J = 25 °C	1.250	1.265	1.280	V
Maximum Switching Frequency	f_{SREQ}	T_J = 25 °C	118	132	145	kHz
OUTPUT VOLTAGE Pin Auto-Restart Threshold	$V_{VO(AR)}$			3.45		V
OUTPUT VOLTAGE Pin Auto-Restart Timer	$t_{VOUT(AR)}$			49.5		ms
BPS Pin Current at No-Load	I_{SNL}	T_J = 25 °C		325	485	µA
BPS Pin Voltage	V_{BPS}		4.20	4.40	4.60	V
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)(TH)}$		3.60	3.80	4.00	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)(H)}$			0.6		V
Current Limit Voltage Threshold	$I_{SV(TH)}$	External Resistor	33.94	35.90	37.74	mV
FWD Pin Voltage	V_{FWD}		150			V
Minimum Off-Time	$t_{OFF(MIN)}$		2.48	3.38	4.37	µs
Soft-Start Frequency Ramp Time	$t_{SS(RAMP)}$	T_J = 25 °C	7.5	11.8	16	ms
BPS Pin Fault Detection Threshold Current	$I_{BPS(SD)}$		5.2	8.9		mA
FEEDBACK Pin Short-Circuit	$V_{FB(OFF)}$			112	135	mV
Thermal Foldback	T_{JB}			124		°C
Thermal Foldback Hysteresis	$T_{JB(H)}$			15		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Synchronous Rectifier @ T_J = 25 °C							
SR Pin Drive Voltage	V_{SR}				4.4		V
SR Pin Voltage Threshold	$V_{SR(TH)}$					0	mV
SR Pin Pull-Up Current	$I_{SR(PU)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz		135	165	195	mA
SR Pin Pull-Down Current	$I_{SR(PD)}$	T_J = 25 °C C_{LOAD} = 2 nF, f_{SW} = 100 kHz		87	97	107	mA
Rise Time	t_R	T_J = 25 °C C_{LOAD} = 2 nF	0-100%		71		ns
			10-90%		40		
Fall Time	t_F	T_J = 25 °C C_{LOAD} = 2 nF	0-100%		32		ns
			10-90%		15		
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 10 mA		7.2	8.3	9.4	Ω
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} = 4.4 V I_{SR} = 10 mA		10.8	12.1	13.4	Ω

Notes:
A. This parameter is derived from characterization.

Typical Performance Curves

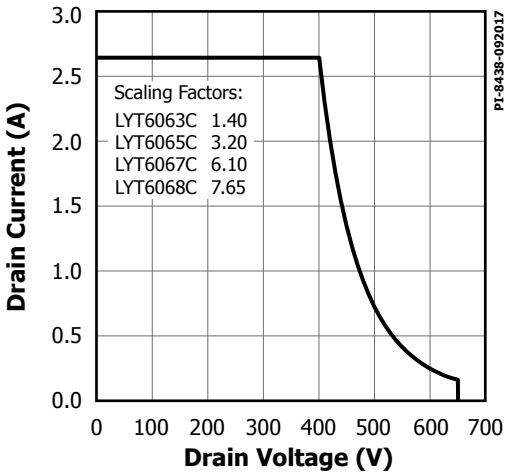


Figure 18. Maximum Allowable Drain Current vs. Drain Voltage.

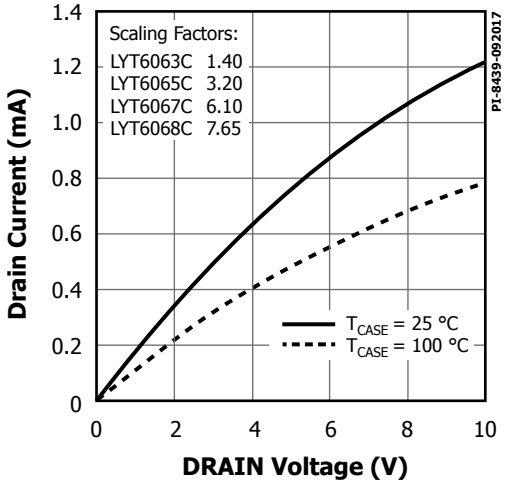


Figure 19. Output Characteristics.

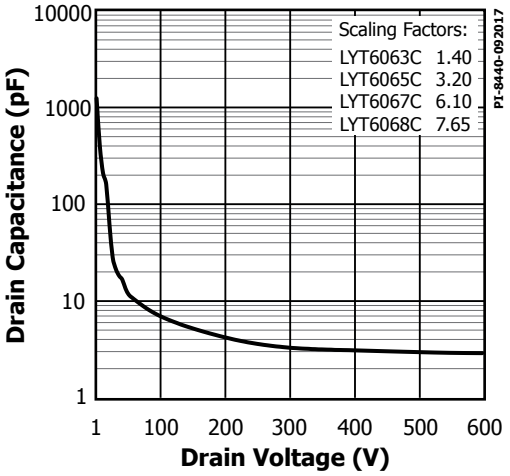


Figure 20. C_{OSS} vs. Drain Voltage.

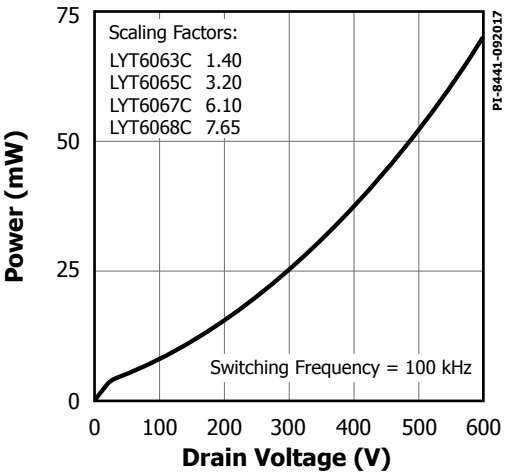


Figure 21. Drain Capacitance Power.

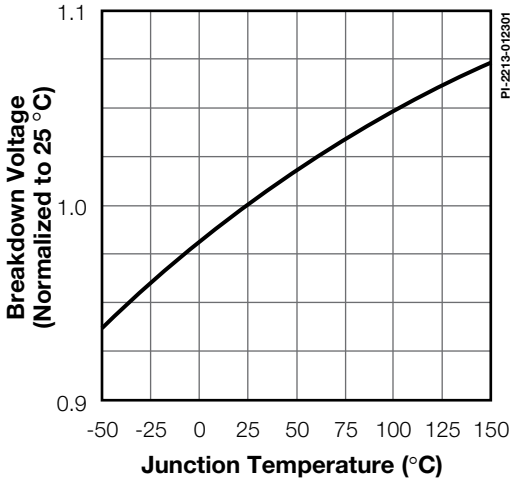


Figure 22. Breakdown vs. Temperature.

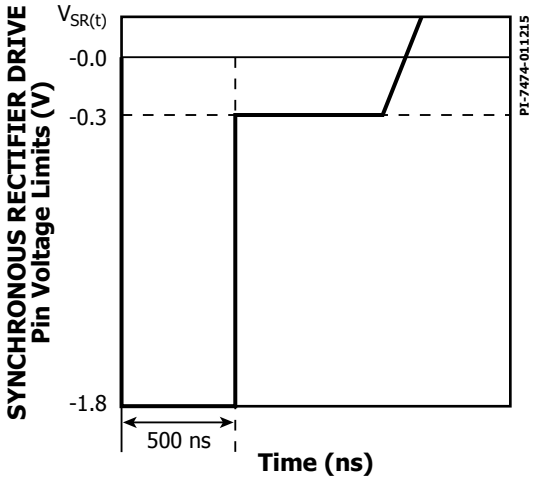


Figure 23. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

Typical Performance Curves

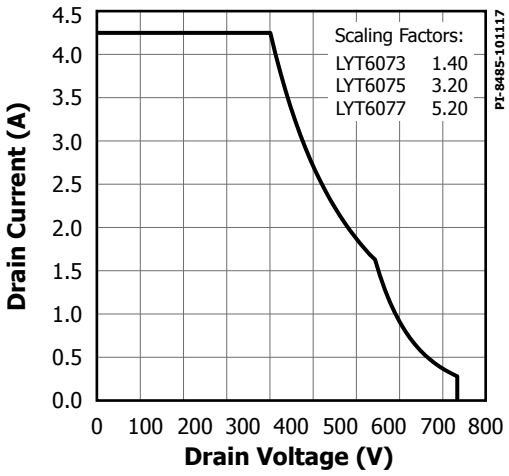


Figure 24. Maximum Allowable Drain Current vs. Drain Voltage.

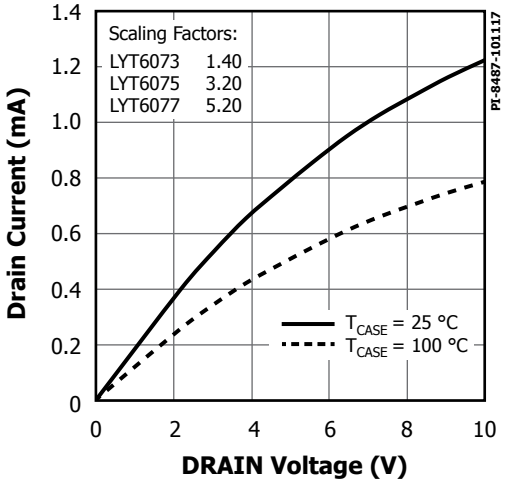


Figure 25. Output Characteristics.

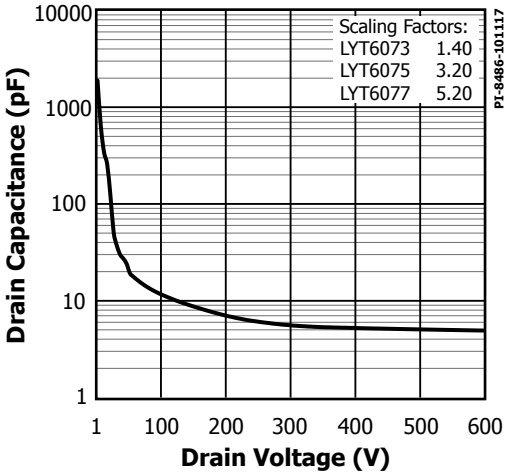


Figure 26. C_{OSS} vs. Drain Voltage.

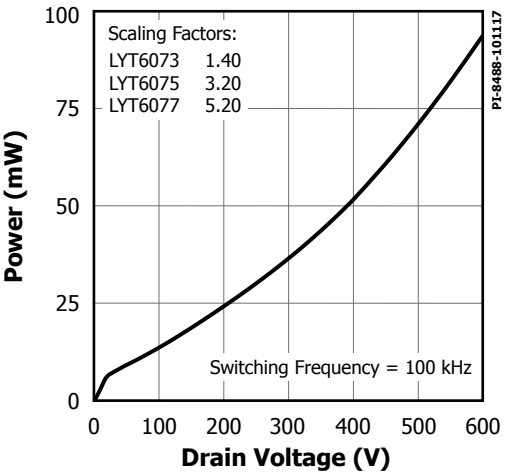
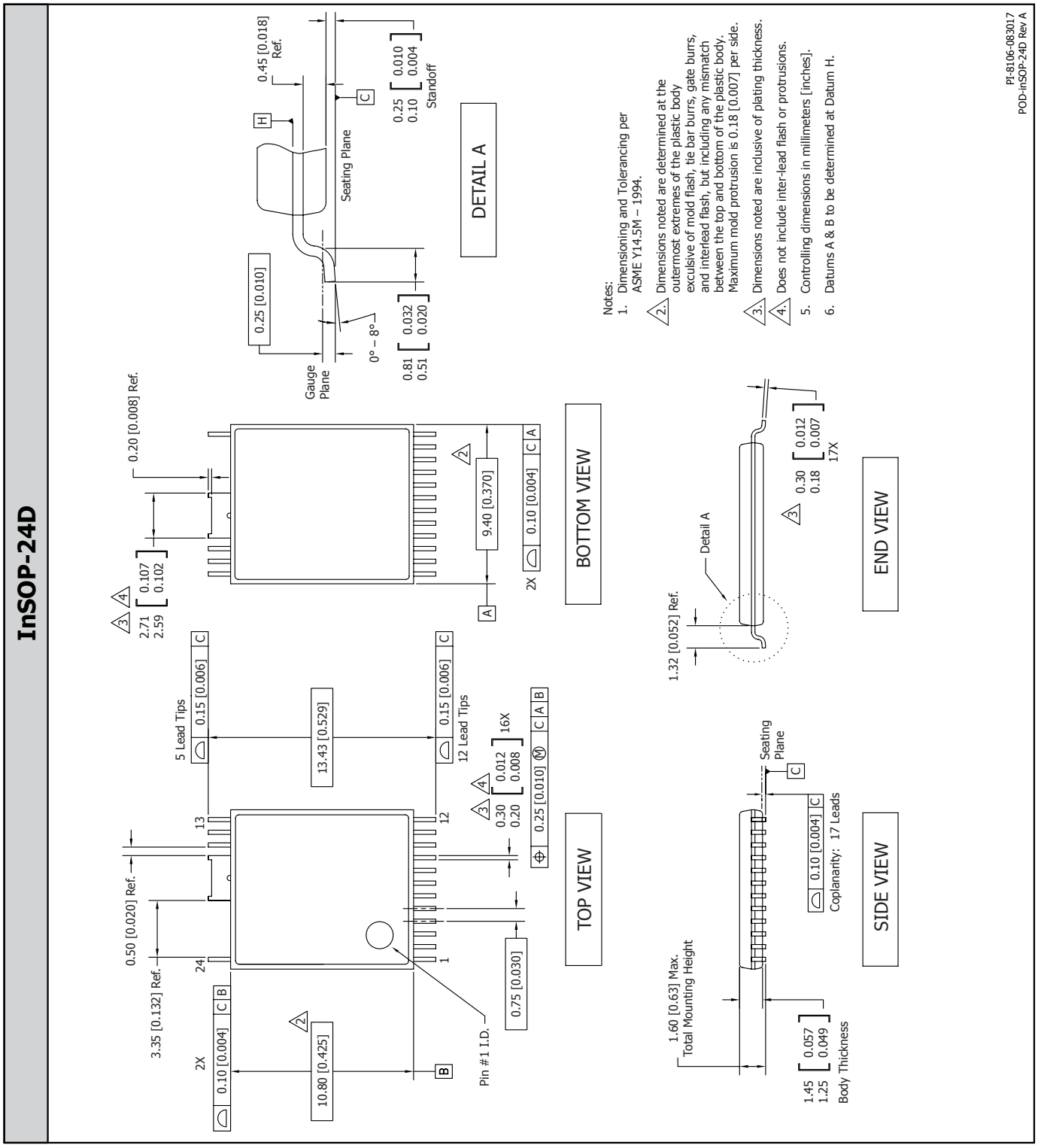


Figure 27. Drain Capacitance Power.

InSOP-24D



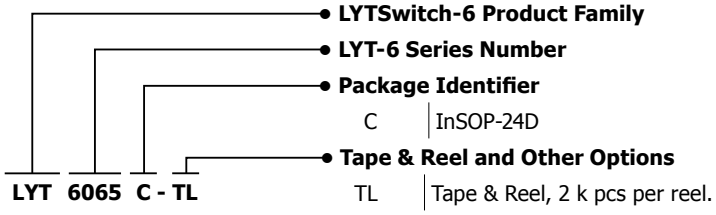
MSL Table

Part Number	MSL Rating
LYT60xxC	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > 1.5 × V_{MAX} on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

Part Ordering Information



Revision	Notes	Date
E	Code L. Added Applications section.	02/18

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